



## Very-Large-Scale Integration Design

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### Editorial

A wafer is a thin slice silicon or germanium material used in electronics for the fabrication of integrated circuits. More often silicon is recommended for wafer selection because it is abundant material and low cost when compare to germanium. Cut in rate voltage of germanium is higher than silicon. Selection process of semiconductor either silicon or germanium is based on requirement. The integration methodology is Small Scale Integration, Medium Scale Integration, Large Scale Integration, Very Large Scale Integration, Ultra Large Scale Integration and System on Chip. The total system is built in a single

chip it is said to be system on chip. VLSI play major role in technology development. The circuit system is partition in to multiple subsystems based on design constraints. Each system which consists number of transistors or transfer resistor which act as logic gate. Design entity is area, speed, power consumption, design time and testability. Nest step which is followed to design entity is logical synthesis which is done over hardware description language like very high speed hardware description language and verification logic. Outcome of simulation is Error identification. By using specific hardware testing is done to identify defects in integrated circuits before product conversion.

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**Received** February 09, 2017; **Accepted** February 16, 2017; **Published** February 23, 2017

**Citation:** Sukumar P (2017) Very-Large-Scale Integration Design. J Electr Electron Syst 6: e120. doi:[10.4172/2332-0796.1000e120](https://doi.org/10.4172/2332-0796.1000e120)

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