Mini Review
Volume 10:6, 2021

International Journal of
Sensor Networks and Data Communications

ISSN: 2090-4886 Open Access

Unity Gain and Variable Gain OTA Buffer Amplifier with Resistive Load Using Multi-Gate Transistors

Remya Jayachandran* and Rama S Komaragiri

Department of Electronics and Communication, The National Institute of Engineering Mysore, Karnataka, India

Abstract

Analog buffer amplifier using reconfigurable FET and gate-all around FET devices are demonstrated to analyze the feasibility of using multi-gate device in analog circuits. In this paper, a unity gain OTA buffer and a simple configuration for a variable gain OTA buffer amplifier are presented. The gain can be varied without changing any other circuit parameters, thus making the configuration more flexible compared to the existing buffer amplifier designs.

Keywords: Buffer amplifier • OTA • Resistive load • SG-RFET • GAAFET

Introduction

Buffer amplifier circuits using operational amplifiers are commonly used as buffer circuits in analog signal processing applications for driving heavy resistive loads. Unity gain buffer amplifier using OTA is the most fundamental driving scheme used in LCD column drivers to drive large capacitive loads [1]. Biomedical, video and telecommunication applications require a buffer amplifier capable of driving heavy resistive loads preferably with a variable gain. DC coupling is required to drive heavy resistive loads (typically below 100 Ω) which complicates the buffer design. While driving a heavy resistive load, a trade-off exists among voltage gain, output swing, and power consumption that sets the performance limits on the existing buffer circuit designs.

The rapid development of smart phones and other electronic gadgets has forced a significant downscaling in the physical size of devices. The increased demand for high-speed, low- power devices and compactible devices has replaced the planar MOSFET with new device architectures and materials. As device dimension shrinks, gate control over the channel of planar transistors becomes more difficult. The conventional planar MOSFETs are replaced by new device architectures such as multi-gate devices, carbon nanotubes, tunnel FETs, single- electron devices, reconfigurable FETs to meet the demands for high speed, compatible and low power consumption [2-9]. Among these, Reconfigurable Field-Effect Transistor (RFET) is an emerging multi-gate device. RFET can be configured as an n-type FET or a p-type FET by applying an appropriate bias to the terminals. Fabrication of the RFET device is less complex compared to the existing MOS transistors, as there is no need for doping.

RFET device structures with triple gate, double gate and single gate are reported in literature [10-14]. A simple and high-performance RFET with a single control gate RFET (SG-RFET) [13]. Compared to triple gate RFET and polarity gate RFET, SG-RFET has a very simple structure. The structure of SG-RFET device is similar to the multigate Device Gate-All-Around FET (GAAFET). In GAAFET, the gate material extends to surround the channel on all sides in order to attain maximum electrostatic integrity. Cylindrical type GAAFET offers the lowest natural length which leads to further scaling of the device. Because of the special architecture of GAA device, carrier conduction is not limited through Si/SiO2 interface but it is through the center of the device. This in turn reduces the interface related issues in device modeling. The device dimensions are gate dielectric thickness (tox), channel length (LG) and channel diameter (tsi).

Digital circuits realized using RFET device is found in literature [8, 15-28]. The results show good performance and is comparable with the other multigate transistors. In, RFET is realized on a planar fully depleted (FD)- SOI device and the electrostatics and the performance of the device are studied and compared with the standard 28 nm FD-SOI [15]. High-frequency analog applications using the double-gate and single-gate RFET [16]. In, reconfigurable circuits using polarity controlled double gate RFET with excellent performance are reported and a two-transistor fully functional XOR gate is demonstrated for the first time [17]. In, inverter circuits based on the Gate All Around FET (GAAFET) with elliptical cross-section are analyzed to observe an improvement in the delay of the circuits compared to a circular cross-section device [18]. In, performance analysis of logic gates using polarity controlled RFET [19, 20].

Experimental demonstration of current mirrors using silicon nanowire transistors in inversion and the sub-threshold region [21]. In, silicon channel is replaced by germanium, which resulted in a low power dissipation due to reduced series resistance [22]. A ring oscillator circuit and in analog and digital circuits implemented using tunnel FET with an astounding performance at low supply voltage [23, 24]. RFET with strained silicon to improve the mobility [25]. The performance analysis of a single gate to triple gate RFET [26]. A top-down fabrication of RFET with symmetric transfer characteristics that exhibits minimal hysteresis, high on- and low off-currents for both, n and p configuration [27]. The electron transport through NiSi2-Si contacts in the RFET [28]. In, current mirrors are demonstrated for the first-time using SG-RFET device with reconfigurable nature [8]. However, the analog circuits using the RFET device are not found in the literature. Buffer amplifier circuit capable of driving resistive loads are required in many analog signal processing applications. Hence, buffer circuit designed using new device architectures - SG-RFET and GAAFET, help to analyses the feasibility of using SG-RFET and GAAFET device in analog circuits.

Unity gain buffer configuration-buffer 1 is implemented using SG-RFET device and GAAFET device and compared with the buffer 1 implemented using OTA IC LM13700 [29]. In this paper, unity gain buffer 2 configurations proposed in and variable gain buffer circuit proposed in with resistive load using SG-RFET device and GAAFET [29, 30].

Unity Gain OTA Buffer Using SG-RFET Inverter and GAAFET Inverter Circuit

The detailed study of the OTA buffer amplifiers using MOSFET [29]. The load driving capability is increased by increasing the gm of OTA. A unity

***Address for Correspondence:** Remya Jayachandran, Department of Electronics and Communication, The National Institute of Engineering Mysore, Karnataka, India; E-mail: remyajayachandran@nie.ac.in*

Received: July 01, 2021; **Accepted:** July 15, 2021; **Published:** July 22, 2021

gain buffer amplifier circuit-buffer 2 using OTA with improved load driving capability and wide bandwidth [29].

Structure of SG-RFET and GAAFET simulated in TCAD Sentaurus is shown in Figure 1 [30]. A two-stage buffer amplifier circuit using OTA is realized using SG-RFET OTA and GAAFET OTA in Sentaurus TCAD tool. Due to the dense meshing at the interface regions in the device, it is difficult to simulate the circuit with more components in Sentaurus TCAD tool. The OTA configuration used in the simulation is Nauta's OTA as it contains only inverter blocks. To minimize the complexity in computation, two-stage buffer 2 configuration is implemented using the non-planar devices- SG-RFET and GAAFET and analyzed the output. Using sdevice module in TCAD, electrical characterization of the two-stage unity gain OTA buffer circuit is carried out with resistive load. Buffer 2 configuration can drive heavy resistance loads as the output impedance of the configuration decreases with the increase in the number of stages N.

The circuit parameters used in the simulation are supply voltage VDD = 2 V, output load resistance, RL = 1 kΩ, input sinusoidal signal amplitude, Vpp = 0.5 V, and frequency 1 kHz. For two-stage buffer 2 using SG-RFET OTA and GAAFET OTA, a peak-to-peak amplitude of 0.495 V is obtained as output from the simulation results, that results in a gain of 0.99 V/V. As the RL reduces, the buffer circuit's gain reduces as expected. The hardware of the two-stage OTA buffer circuit is implemented using OTA LM13700 IC and verified the performance. Depicts the simulation results of buffer 2 configuration implemented using different OTAs (Table 1). The performance of the SG-RFET OTA buffer amplifier is compared with GAAFET OTA and CMOS OTA. GAAFET buffer 2 configuration exhibits a wide bandwidth compared to other configurations.

Variable Gain Analog Buffer Amplifier

The OTA based unity gain analog buffer amplifier circuit is modified by applying a feedback voltage as shown in Figure 2. Tunable gain OTA buffer amplifier is presented in using CMOS OTA [29]. In this section, design of a simple variable gain buffer amplifier implemented using SG-RFET, GAAFET OTA and OTA IC LM13700 are presented.

The feedback factor of the buffer configuration is:

$G_L = g_o + g_L$ (1)

$B = 1/A_v - GL/g_m$ (2)

Here go, B, Av are output conductance, feedback factor and gain respectively. The feedback factor depends on the gain and the output load of the proposed configuration. Shows the variation in gain with respect to the feedback factor with a 1 kΩ as the output load (Figure 3) [30].

The feedback circuit is implemented using the buffer 1 with a resistive load to obtain the required feedback voltage. The desired gain is achieved by varying the feedback voltage. The feedback factor depends on both the gain and output load that reduces the maximum output swing. The design simplicity makes the proposed configuration useful in biomedical, video and telecommunication applications. The limitation of this configuration is its low input dynamic range, and the area requirement for large gm OTAs to drive low-resistance load. In this work, the functionality of the buffer circuit is verified using the OTA IC-LM13700 [9]. The gain variation with respect to

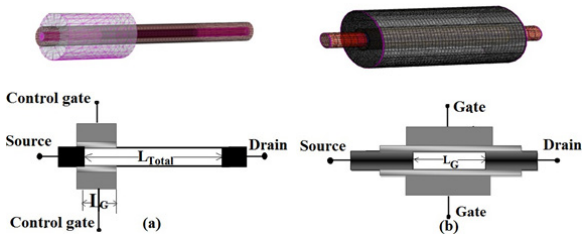

Figure 1. a) Structure of SG-RFET and b) GAAFET simulated in Sentaurus TCAD.

		Unity gain amplifier- two OTA		
Parameters	**LM13700 IC**	**GAAFET OTA**	**SG-RFET OTA**	**Strained silicon SG-RFET OTA**
Supply voltage	±15 V	2	2	2
gm (mS)	9.6	1	0.79	0.9
RL (kΩ)	10	1	1	1
Bandwidth (MHz)	0.81	5000	510	720
Gain (V/V)	0.99	0.99	0.99	0.99

Table 1. Two-stage buffer 2 configuration with resistive load.

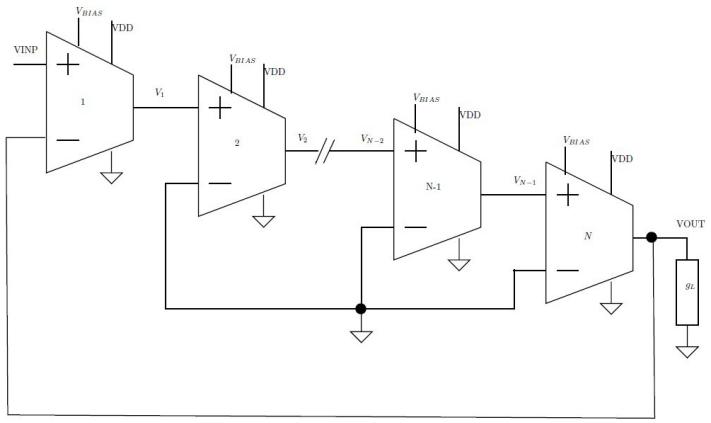

Figure 2. N-stage OTA buffer amplifier circuit..

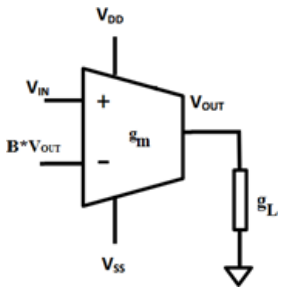

Figure 3. Variable gain OTA buffer circuit.

changes in feedback voltage is observed at a particular resistance load. represents the circuit parameters of the OTA IC -LM13700, GAAFET-OTA and this work (Table 2). The proposed circuit is implemented using OTA LM13700 IC.

Depicts the circuit parameters of the different OTA buffer amplifiers. The tunable gain represents the maximum gain possible for the proposed buffer configuration. Shows the buffer amplifier circuit parameters used in simulations.

The simple design, low fabrication complexity, reconfigurable property and reduced area make SG-RFET outperform the existing devices. The trade-off is speed and supply voltage. Supply voltage greater than 1.5 V is required to obtain high ION /IOF F ratio. By using SiGe or Germanium instead of silicon, the drain current of an SG-RFET can be improved thus enabling low voltage operation [31]. Compared to SG-RFET OTA buffer circuits, GAAFET OTA buffer has wide bandwidth (Figure 4).

Variable gain buffer amplifier using OTA				
Parameters	**LM13700 -OTA IC (Hardware)**	**GAAFET OTA**	**SG-RFET OTA**	**Strained silicon SG-RFET OTA**
Power supply (V)	15	2	2	2
gm (mS)	9.6	1	0.79	0.9
RL (kΩ)	10	1	1	1
Bandwidth (MHz)	0.8	4800	360	550
Tunable gain (V/V)	up to 8	up to 5	up to 4	up to 5

Table 2. Buffer amplifier circuit parameters.

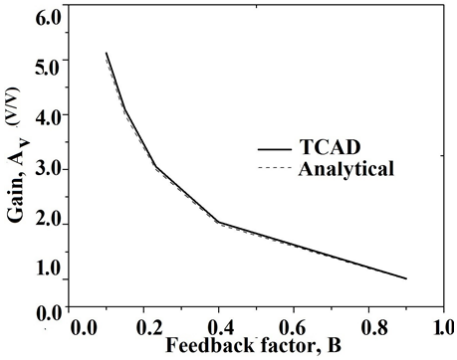

Figure 4. Variable gain OTA buffer circuit.

Conclusion

In this paper, two-stage buffer 2 configuration and a simple OTA buffer amplifier circuit with a variable gain is presented. The OTA buffer is implemented with SG-RFET OTA and GAAFET OTA in Sentaurus TCAD, and the simulation results and functionality are verified using the LM13700 OTA IC. Hardware implementation of the simple variable gain buffer circuit is carried out using the LM13700 OTA IC to verify the functionality of the circuit. SG-RFET buffer amplifier exhibits good characteristics with a gain tunability of up to 5 V/V for 1 kΩ load. GAAFET buffer circuit has a wide bandwidth and gain tunability up to 5 V/V for 1 kΩ load. Variable gain buffer amplifier circuit using the SG-RFET device and GAAFET device indicate the design flexibility on analog circuits in analog signal processing applications.

References

1. Sawigun, Chutham, Andreas Demosthenous, Xiao Liu and Wouter A. Serdijn. "A Compact Rail-To-Rail Class-Ab CMOS Buffer with Slew-Rate Enhancement." *IEEE Trans Circuits Syst II Express Briefs* 59 (2012): 486-490.
2. Singh, Amandeep, Mamta Khosla and Balwinder Raj. "Design and Analysis of Electrostatic Doped Schottky Barrier CNTFET Based Low Power SRAM." *AEU Int J Electron Commun* 80 (2017): 67-72.
3. Hosseini, Khadem Vahideh, Daryoosh Didebana, Mohammad Taghi Ahmadi and Razali Ismail. "An Analytical Approach to Model Capacitance and Resistance of Capped Carbon Nanotube Single Electron Transistor." *AEU-Int J Electron Commun* 90 (2018): 97-102.
4. Lin, Yu-Ming, Joerg Appenzeller, Joachim Knoch and Phaedon Avouris. "High-Performance Carbon Nanotube Field-Effect Transistor with Tunable Polarities." IEEE Trans NanoTechnol 4 (2005): 481-489.
5. Heinzig, Andre, Stefan Slesazeck, Franz Kreupl and Thomas Mikolajick, et al. "Reconfigurable Silicon Nanowire Transistors." *Nano Letters* 12 (2011): 119-124.
6. Ahmad, Sayeed, Naushad Alam and Mohd Hasan. "Robust TFET SRAM Cell for Ultralow Power IoT Applications." *AEU-Int J Electron Commun* 89 (2018): 70-76.
7. Jayachandran, Remya, Rama S Komaragiri and P C Subramaniam. "Study Of Circuits Based on SOI-Vertical Gate-All-Around FET." *IEEE India Counc Int Conf* 1 (2018): 1-6.

8. Jayachandran, Remya, Rama S Komaragiri and P C Subramaniam. "Reconfigurable Circuits Based on Single Gate Reconfigurable Field-Effect Transistors." *IEEE Int Conf Electron Comput Commun Technol* 1 (2020): 1-5.

9. Texas Instruments. "LM13700 Datasheet."

10. Weber, M. Walter, Lutz Geelhaar, Luca Lamagna and Marco Fanciulli, et al. "Tuning the Polarity of Si-Nanowire Transistors without the Use of Doping." *IEEE Conf NanoTechnol* 08 (2008): 580-581.

11. Wessely, Frank, Tillmann Krauss and Udo Schwalke. "CMOS Without Doping: Multigate Silicon-Nanowire Field-Effect-Transistors." *IEEE J Solid State Circuits* 70 (2012): 33-38.

12. Sacchetto, Davide, Yusuf Leblebici and Giovanni De Micheli. "Ambipolar Gate-Controllable SiNW FETs for Configurable Logic Circuits with Improved Expressive Capability." *IEEE Electron Device Lett* 33 (2012): 143-145.

13. Darbandy, Ghader, Martin Claus and Michael Schröter. "High-Performance Reconfigurable Si Nanowire Field-Effect Transistor Based on Simplified Device Design." *IEEE Trans NanoTechnol* 15 (2016): 289-294.

14. Rajan, Ranjith, Remya Jayachandran, K. Suja and Rama Komaragiri. "Two-Dimensional Analytical Model for A Reconfigurable Field Effect Transistor." *Superlattices Microstruct* 114 (2018): 62-74.

15. Navarro, Carlos, Sylvain Barraud, S. Martinie and Joris Lacord, et al. "Reconfigurable Field Effect Transistor for Advanced CMOS: Advantages and Limitations." *IEEE J Solid-State Circuits* 128 (2017): 155-162.

16. Darbandy, Ghader, Martin Claus and Michael Schröter. "Optimization of Reconfigurable Si-NW FETs for Analog High-Frequency Applications." *Int Conf Simul Semicond Process Devices* 1 (2016): 245-248.

17. Marchi, De M, Davide Sacchetto, Stefano Frache and Pierre-Emmanuel Gaillardon, et al. "Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs." *IEEE Int Electron Devices Meet* 1 (2012): 8-4.

18. Kumar, Subindu and Shankaranand Jha. "Impact of Elliptical Cross-Section on the Propagation Delay of Multi-Channel Gate-All-Around MOSFET Based Inverters." *Microelectronics J* 44 (2013): 844-851.

19. Marchi, De M, Jian Zhang, Stefano Frache and Davide Sacchetto, et al. "Configurable Logic Gates Using Polarity-Controlled Silicon Nanowire Gate-All-Around FETs." *IEEE Electron Device Lett* 35 (2014): 880-882.

20. Gaillardon, Emmanuel-Pierre, Luca Amaru, Jian Zhang and Giovanni De Micheli. "Advanced System on A Chip Design Based on Controllable-Polarity FETs." *Proc Conf Des Autom Test Eur* 235 (2014): 1-6.

21. Huang, Ru, Jibin Zou, Runsheng Wang and Chunhui Fan, et al. "Experimental Demonstration of Current Mirrors Based on Silicon Nanowire Transistors for Inversion and Subthreshold Operations." *IEEE Trans Electron Devices* 58 (2011): 3639-3642.

22. Wang, Dunwei, Bonnie A Sheriff and James R Heath. "Complementary Symmetry Silicon Nanowire Logic: Power-Efficient Inverters with Gain." *Small* 2 (2006): 1153-1158.

23. Qiu, Xiaohui, Dihu Chen and Zixin Wang. "Response of Ring Oscillator to Periodic Interference on The Power Supply." *AEU-Int J Electron Commun* 82 (2017): 383-390.

24. Strangio, Sebastiano, Marco Lanuzza, Felice Crupi and Luca Selmi, et al. "Digital and Analog TFET Circuits: Design and Benchmark." *Solid-State Electron* 146 (2018): 50-65.

25. Heinzig, Andre, Thomas Mikolajick, Jens Trommer and Daniel Grimm, et al. "Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport." *Nano Lett* 13 (2013): 4176-4181.

26. Moura, Rebeca, Nils Tiencken, Sven Mothes and Martin Claus, et al. "Reconfigurable NanoFETs: Performance Projections for Multiple-Top-Gate Architectures." *IEEE Trans NanoTechnol* 17 (2018): 467-474.

27. Simon, Miak, Boshen Liang, Dustin Fischer and Martin Knaut, et al. "Top-Down Fabricated Reconfigurable FET with Two Symmetric and High-Current On-States." *IEEE Electron Device Lett* 41 (2020): 1110-1113.

28. Fuchs, Florian, Sibylle Gemming and Jorg Schuster. "Electron Transport Through NiSi2-Si Contacts and Their Role in Reconfigurable Field-Effect Transistors." *J Phys Condens Matter* 31 (2019): 355002.

29. Jayachandran, Remya, P. C. Subramaniam and K. J. Dhanaraj. "A Novel Tunable Gain CMOS Buffer Amplifier for Large Resistive Loads." *Integration* 77 (2021): 1-2.

30. Jayachandran, Remya, Rama Komaragiri and P C Subramaniam. "High-Performance Reconfigurable FET for A Simple Variable Gain Buffer Amplifier Design." *Int J Electron* 2021.

31. Trommer, Jens, Andre Heinzig, Stefan Slesazeck and Uwe Muhle, et al. "Reconfigurable Germanium Transistors with Low Source-Drain Leakage for Secure and Energy-Efficient Doping-Free Complementary Circuits." *Annu Device Res Conf* 1 (2017): 1-2.

How to cite this article: Jayachandran, Remya and Rama S Komaragiri."Unity Gain and Variable Gain OTA Buffer Amplifier with Resistive Load Using Multi-Gate Transistors."*J Sens Netw Data Commun* 10 (2021): 131.