

Editorial

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# Time-Mode Approach for Mixed Analog-Digital Signal Processing

## Guangyu Zhu, Fei Yuan\* and Gul Khan

Department of Electrical and Computer Engineering, Ryerson University, Toronto, Ontario, Canada

#### Abstract

Time-mode circuits where information is represented by the timing difference of digital signals possess a number of intrinsic characteristics that are scaled well with CMOS technology, making them a promising and viable option to implement some of the key building blocks of mixed analog-digital subsystems Analog-to-Digital Converters (ADCs) and Phase-Locked Loops (PLLs). This paper examines the challenges encountered in analog design with technology scaling and presents the fundamental advantages of time-mode circuits. It investigates the building blocks of time-mode circuits for mixed analog-digital signal processing with a special focus on ADCs.

## Introduction

The rapid advance of CMOS technologies has primarily been geared towards the optimal performance of digital systems. As a result, analog circuits are not only losing the benefit of specialized and process-controlled components; they must also cope with aggressively decreasing voltage headroom caused by the slow decline of device threshold voltage and rapid reduction in supply voltage while meeting ever-demanding performance specifications [1-3]. The shrinking voltage headroom not only increases voltage error and deteriorates signal-to-noise ratio, it also worsens the effect of the nonlinear characteristics of MOS transistors and reduces dynamic range of voltagemode circuits. Current-mode approaches offer an alternative means to cope with voltage headroom loss. The need for low-impedance nodes throughout current-mode circuits, however, is accompanied with large branch currents subsequently high power consumption [4]. As a result, current-mode circuits are primarily used in applications where speed rather than power is of the most critical concern such as I/Os. The detrimental effect of technology scaling on the performance of analog circuits can be compensated to a certain degree using digitally-assisted means, this, however, is at the cost of increased circuit complexity and high power consumption [5,6].

The intrinsic gate delay of digital circuits, on the other hand, is the primary beneficiary of technology scaling. The improved switching characteristics of MOS transistors offer an excellent timing accuracy such that the time resolution of digital circuits has well surpassed the voltage resolution of analog circuits. A new design paradigm where information is represented by the duration of pulses, i.e., time, rather than analog nodal voltages or branch currents of electric networks, offers a new means to combat the challenges that once seemed unconquerable in analog domain. Unlike voltage-mode circuits that represent information using nodal voltages or current-mode circuits that quantify information using branch currents, time-mode circuits depict an analog signal with a time difference between two digital signals with the time difference linearly proportional to the amplitude of the analog signal. Since information is represented by the time difference of digital signals, time-mode circuits perform analog signal processing in the digital domain without using power-greedy and speed-impaired digital signal processors. As a result, not only the performance of time-mode circuits scales well with technology, a distinct and intrinsic characteristic of time-mode circuits, time-mode circuits also offer high-speed signal processing with low power consumption. This paper briefly examines the challenges encountered in analog design with technology scaling and investigates the intrinsic advantages of timemode signal processing. The building blocks of time-mode circuits and their design constraints are studied. The application of time-mode circuits in analog-to-digital converters is the focus of this paper.

#### Voltage-To-Time Converters

One of the key building blocks of time-mode circuits is Voltageto-Time Converters (VTC) that map an analog voltage to a time difference variable, i.e., a pulse whose width is linearly proportional to the amplitude of the voltage. Once the input voltage is converted to a time-difference variable, time-mode units such as time amplifiers, time adders, time integrators, time differentiators, and Time-to-Digital Converters (TDC) can be utilized for signal processing. VTCs are typically implemented using a Voltage-Controlled Delay Unit (VCDU) with a reference signal with which the input signal is compared from a timing ring Voltage-Controlled Oscillator (VCO) [7]. The VCDU can be generally categorized into direct VCDU and current-starved VCDU [8-10]. The former uses a constant current source to charge a capacitor during the sampling period and a current-steering amplifier to sense the difference between the input voltage and the capacitor voltage [11]. The latter, which is more common in recent designs, adjusts the delay of a current-starve inverter using the sampled input. The time difference between the edge of the reference signal generated by the reference VCO and that of the VCDU is directly proportional to the sampled input and is the time-mode representation of the sampled input voltage. Direct VCDUs offer a high conversion gain and a large dynamic range but suffer from limited bandwidth and high power consumption. Currentstarved VCDUs, on the other hand, features a small conversion gain, a large bandwidth, and consume less power.

#### Time-To-Digital Converters

TDCs convert a time-difference variable to a digital code [6,7]. The use of TDCs in nuclear science research dates back to 1970s [12,13]. The applications of TDCs, however, has extended well beyond nuclear

\*Corresponding author: Fei Yuan, Department of Electrical and Computer Engineering, Ryerson University, Toronto, Ontario, Canada, E-mail: fyuan@ryerson.ca

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science to digital storage oscillators [14,15], laser range finders [16], digital frequency synthesizers [17], and analog-to-digital converters [18], to name a few. TDCs can be loosely classified to analog TDCs that perform time-to-digital conversion using intermediate quantities other than time such as currents and charge and digital TDCs that quantize a given time interval by counting the number of the transitions of the reference clock in the sampling interval. The former include singleslope TDCs and dual-slope TDCs while direct-counter TDCs are the representative of the latter. Analog TDCs are largely used in low-speed applications primarily due to their long conversion time. Although direct-counter TDCs have a large dynamic range with the upper bound set by the size of the counter and a superior linearity, the resolution of direct counter TDCs is limited by the reference clock. To improve the resolution, a high-frequency clock is needed. This is accompanied with high power consumption and increased crosstalk. To quantify a small time interval, delay-line TDCs with a START pulse propagating through the delay line and a STOP pulse disabling the D Flip-Flops that sample the output of the delay stages can be used. Clearly, the dynamic range of delay-line TDCs is determined by the length of the delay line. The linearity of delay-line TDCs is set by the delay mismatch of delay stages. The resolution of direct-counter TDCs can be improved to the gate delay without increasing the reference clock frequency. This is achieved by using delay lines that quantize the timing error between the rise and fall edges of the time interval to be measured and the edge of the reference clock. We term these TDCs counter/delay-line TDCs [6,18]. The linearity of counter/delay-line TDCs is determined by the stability of the reference clock and the delay mismatch of the delay stages. Resolution can be doubled if both the rise and fall edges of the delay stages are utilized [19]. To further improve the resolution to subgate delay, interpolation between the edges of adjacent delay stages can be utilized [20,21]. Another technique to achieve the resolution of subgate delay is to use an array of Delay-Locked Loops (DLLs) [22]. Since the time delay of delay lines is subject to the effect of process spread, temperature variation, and voltage fluctuation (PVT), a DLL locked to a clean reference is typically mandatory to minimize the effect of PVT.

TDCs with a virtually unlimited resolution can be obtained using Vernier delay lines where START and STOP pulses whose time difference is to be measured propagate in two separate delay lines of different delays. The delay line in which START pulse propagates, thereafter called START-line, has a slightly longer delay and the delay line in which STOP pulse propagates (STOP-line) has a slightly shorter delay [23]. Since the delay of the START-line is smaller, STOP pulse propagating in the STOP-line will catch up with START pulse in the START-line. When this occurs, the time-to-digital conversion is completed and the resultant digital code is given by the output of the delay stages. Clearly, the dynamic range of Vernier line TDCs is set by the length of the lines. Although theoretically the resolution of Vernier-line TDCs can be infinitely small, in reality, it is limited by the delay mismatch of the delay stages. Vernier-line TDCs suffer from an increased hardware cost due to the need for two delay lines and a limited dynamic range set by the length of the delay lines. A large dynamic range can be obtained if Vernier delay lines are used in conjunction with counters, similar to the counter/delay-line TDCs investigated earlier. The performance of Vernier-line TDCs can also be improved using a two-level Vernier-line technique proposed in [24].

To increase the dynamic range of TDCs, pulse-shrinking TDCs that uses skewed delay stages, i.e., the delay stages with propagation delay larger than that of the rest delay stages, in a cyclic delay line to reduce the width of the pulse propagating in the delay line can be used [25]. In this configuration, the pulse propagates in a ring of regular delay stages and a skewed delay stage until the pulse diminishes. A counter is used at the end of the ring to record the number of the round trips that the pulse makes. The content of the counter when the pulse diminishes in the ring is the digital representation of the pulse width. Clearly, the resolution of cyclic pulse-shrinking TDCs is the delay of the loop. Pulse-shrinking TDCs enjoy a large dynamic range as the upper bound is set by the size of the counter. Another intrinsic characteristic of cyclic pulse-shrinking TDCs is the absence of the effect of nonlinearities as the input pulse must propagate through the entire delay line to increment the counter. As a result, the amount of cycle-to-cycle pulse shrinking remains unchanged. A drawback of cyclic pulse-shrinking TDCs is the latency needed for the pulse to diminish completely before another pulse can be applied to the ring to avoid signal collision [21]. Another drawback of pulse-shrinking TDCs including cyclic pulse-shrinking TDCs is the effect of temperature on the loop delay, which could be as high as 25% over a 100 C temperature range [15]. Note that in delayline TDCs, the effect of PVT on delay is minimized using a DLL locked to a clean reference. This approach, however, has not been applied to cyclic pulse-shrinking TDCs.

Pulse-shrinking TDCs is effective if pulse width is large. When pulse width is small, pulse-stretching TDCs can be utilized to quantize the pulse [15]. Alternatively, one can also uses a time amplifier to stretch the pulse prior to time-to-digital conversion, similar to a voltage amplifier that enlarges a small voltage before voltage-to-digital conversion, in order to achieve a better resolution [26].

## **Time Amplifiers**

Time amplifiers, also known as time difference amplifiers, amplify the width of a given time interval. Time amplifiers that are based on the metastability of SR-latches proposed by Abas [26] and further investigated in [27,28] can have a resolution of 10 ps [26]. The SR-latch time amplifier proposed by Lee and Abidi offers a resolution of 1.25 ps in 90 nm CMOS [29]. A main drawback of SR-latch time amplifiers is that the gain of the amplifiers is set by the characteristics of the latch and is prone to the effect of PVT. Other drawbacks of this type of time amplifiers include a small input range and poor gain nonlinearity. The DLL-based time amplifier proposed in [30] uses a closed-loop approach to minimize the effect of PVT. A similar design was reported in [31]. The need for the establishment of the lock state of DLL of this approach limits their usefulness in applications where conversion speed is critical. In [32,33] a closed-loop time amplification scheme was proposed. The two pulses whose time difference is to be amplified propagate in the opposite directions in two separate delay lines of the same length. The delay of the delay stages is stabilized against the effect of PVT via a DLL locked to a clean reference. Time amplification can also be done by charging a pair of capacitors with two digital signals whose time difference is to be measured, and then sensing the voltage difference of the charged capacitors using voltage comparators [34,35]. The time amplifier proposed by Kim et al. [36] utilizes a simple logic operation to achieve 3.75 ps resolution in 65 nm CMOS. Since the implementation is completely open-loop, its performance is sensitive to device imperfection.

## **Time Quantizers**

Time quantizers can be realized using a time comparator with the reference with which the input is compared from a timing Voltage-Controlled Oscillator (VCO) with fixed frequency and the signal from a sensing VCO whose frequency varies with the sampled input, the need for two VCOs and only single-bit quantization resolution, however, make it less attractive. VCO-based quantizers, on the other hand,

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quantize an input voltage by utilizing one-to-one mapping between the sampled control voltage (the signal) and the frequency of the VCO [37]. Multi-stage ring VCOs are preferred in these applications due to their large frequency tuning range, low power consumption, low silicon cost, high oscillation frequency subsequently fast conversion, digital outputs, multi-bit quantization, and most importantly full compatibility with technology scaling. Single-phase VCO-based quantizers use a counter to record the number of the transitions of the output of the VCO in one sampling period. To lower the quantization error, Kim and Cho used a phase detector to quantify the residue phase, i.e., the phase difference between the sampling clock and the VCO [38]. Multiphase VCO-based quantizers increase quantization resolution by a factor of N where N is the number of the stages of VCOs [38-41]. These quantizers are inherently multi-bit quantizers. Phase interpolation was also utilized to reduce quantization errors [42]. The resolution of VCObased quantizers cannot be increased simply by adding more delay stages alone as the resolution is a logarithmic function of the dynamic range of VCO frequency. The more stages are integrated, the lower the frequency of the VCO subsequently the smaller the dynamic range [38]. To minimize the effect of the nonlinearity of frequency tuning characteristics of ring VCOs, Yoon et al. [43], proposed a dual-VCO approach where two identical VCOs are used to sample a differential input and the output of the counter for each VCO is subtracted to remove even-order harmonics [40]. Matching two VCOs, however, is not a trivial task.

### **Time-Mode Analog-To-Digital Converters**

Driven by the benefits of time-mode signal processing, analog-todigital conversion in time-mode has received an increasing attention from both academia and industry recently. Architecturally, time-mode Analogto-Digital Converters (ADCs) can be loosely categorized into open-loop ADCs and closed-loop ADCs. The former directly perform analog-to-digital conversion in an open-loop fashion while the latter employ negative feedback to improve performance. An open-loop time-mode ADC typically consists of a VTC where the input voltage is sampled and converted to a pulse whose width is proportional to the amplitude of the sampled input and a TDC where the pulse width is digitized [44]. Due to the absence of a self-correction mechanism, open-loop time-mode ADCs enjoy short conversion time and low power consumption. Its performance, however, is severely affected by the nonlinearity of the VTC, and the resolution and nonlinearity of the TDC [45,46]. As a result, these ADCs typically have a poor SNR and a small SNDR. Although a large linear frequency tuning range of VCOs is wanted to improve SNR and SNDR of ADCs with VCO-based quantizers, increasing linear frequency tuning range of ring VCOs is rather difficult. Alternative means are critically needed. As pointed out earlier that dual-VCO TDCs can effectively remove even-order harmonics [40,43].

It is well understood that  $\Sigma\Delta$  modulators offer the key characteristic of noise-shaping, allowing in-band white noise to be pushed to unwanted bands and removed using decimation filters in a postprocessing step. A key characteristic of VCO-based quantizers is their intrinsic first-order noise-shaping [37]. The placement of VCOs inside the feedback loop of  $\Sigma\Delta$  modulators ensures that the control voltage of VCOs is kept small by the negative feedback. As a result, even though ring VCOs exhibit a poor linearity over a large frequency range, the linearity can be significantly improved if the variation of the control voltage of VCO is small, as demonstrated by Straayer and Perrott [47]. Another key advantage of VCO-based quantizers is their intrinsic multi-bit quantization. It is well understood that the performance of multi-bit  $\Sigma\Delta$  modulators is critically affected by the linearity of multibit DACs in voltage domain. The multi-bit DAC proposed in [47] overcomes this difficulty elegantly. Lastly,  $\Sigma\Delta$  modulators with a VCObased quantizer are inherently Continuous-Time (CT)  $\Sigma\Delta$  modulators as the sampling takes place at the VCO rather than outside the feedback loop. Since the input is sampled after it passes the low-pass loop filter preceding the quantizer, the filter acts as an anti-aliasing filter that effectively suppresses aliasing noise [48,49]. As a result, the need for an anti-aliasing filter preceding  $\Sigma\Delta$  modulators is removed. With a highgain loop filter preceding and a 1st-order noise-shaping VCO-based quantizer with Dynamic Element Matching (DEM) in the forward path, time-mode  $\Sigma\Delta$  modulators are capable of providing high-order noise-shaping to improve high SNR and SNDR. For example, the 2<sup>nd</sup>order CT-  $\Sigma\Delta$  modulator with 5-bit VCO-based quantizer proposed in [47,50] achieves SNR and SNDR of 86 dB and 72 dB, respectively, with 10 MHz signal bandwidth and total power consumption of 40 mW. The CT-  $\Sigma\Delta$  modulator with a 4<sup>th</sup>-order loop filter and a 5-bit VCO-based quantizer reported in [48,49] achieves SNR and SNDR of 81 dB and 78 dB, respectively, with 20 MHz signal bandwidth and total power consumption of 87 mW. The 1<sup>st</sup>-order  $\Sigma\Delta$  modulator proposed in [5] employs a 1-bit VCO-based quantizer. No integrator was used. The solo noise shaping is provided by the VCO. The absence of active loop filters greatly lowers the power consumption of the modulator to 0.8 mW yet the ADC achieves SNR and SNDR of 60 dB and 54 dB, respectively with OSR of 348 and signal bandwidth 125-400 kHz. Another family of  $\Sigma\Delta$  modulators employ a Pulse Width Modulation (PWM) generator to convert an analog signal to a pulse and then digitize it using a TDC [51-53]. Since a loop filter proceeds PWM generator and sampling takes place inside the loop, these modulators are also inherently CT- $\Sigma\Delta$  modulators. As compared with  $\Sigma\Delta$  modulators with VCO-based quantizers, the order of noise shaping of TDC-Based  $\Sigma\Delta$  modulators is lower by one. As a result, their SNR and SNDR are poorer as compared with those of  $\Sigma\Delta$  modulators with VCO-based quantizers.

#### Conclusions

In this communication, we have investigated the challenges encountered in analog design with technology scaling and the intrinsic advantages of time-mode approach for mixed analog-digital signal processing. The state-of-the-art of the building blocks of time-mode circuits for mixed analog-digital signal processing has been presented and the design constraints of each of these building blocks have been studied in detail. Time-mode approach offers a promising and viable means to implement mixed analog-digital subsystems such as ADCs and PLLs that scale well with technology.

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