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Surface Defect Classification in Silicon Wafer Manufacturing Using Linear-Based Channeling and Rule-Based Binning

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Abstract

Surface defect control is the serious science in semiconductor industry. Surface defects found at the end product of silicon wafer manufacturing are generated by human, fab facility, equipment and process. Generally, the surface defects found on a silicon wafer could be classified as grown-in Crystal Originated Particles (COPs), Surface-Adhered Foreign Particles (SFPs), and Process-Induced Defects (PIDs). Making the correct defect classification by the surface scanning instrument is of paramount because it provides the opportunity for finding defect root cause, which is part of yield enhancement process. This article reveals a novel defect classification approach by optimizing the linear-based channeling and rule-based binning algorithms applied in KLA surface scanning counter, a commercially available surface defect metrology tool.

Keywords: PID/Process-induced defect • Linear-based channeling • Surface defect • LPD/Light point defect • LPDN/Non-cleanable light point defect • Rule-based binning

Introduction

Silicon material is one of the most common materials using in semiconductor industry due to its good performance in terms of material structure, mechanical strength, chemical and electrical stabilities. A good defect control on silicon material is inevitable and a good surface defect metrology is unavoidable in the silicon wafer manufacturing. There are three types of surface defects defined in the silicon wafer manufacturing, according to the source of those defects.

- Crystal grown-in defect such as the Crystal Originated Particles (COPs), that is the vacancy type of point defect delineated on the wafer surface which impacts the quality of device performance the most, for instance, causing Gate Oxide Integrity (GOI) failure.
- Surface-adhered Foreign Particles (SFPs) which is the organic particle or the metal contaminants generated by human, fab facility, equipment, and process.
- Process-Induced Defects (PIDs), also called Polishing-induced defects. Any kinds of unwanted imperfections generated from the process of silicon wafer manufacturing especially the polishing process, for instance residues, stains, dimple, scratch, surface particles. PIDs dominants gate dielectric failure in the device fabrication process.

By understanding of the source of a defect, defect engineers are able to streamline the process of troubleshooting. It is of fundamental importance for defect engineering in the industry of silicon wafer manufacturing [1].

Defect engineering flow for surface defect metrology

There are five process steps in the flow of defect engineering for surface defect metrology as shown in Figure 1. Defect detection and sizing is the use of laser scanning counter for capturing and sizing the defects on the wafer surface. A beam of an incident light from a laser source is travelled to the wafer surface as to illuminate both the surface and imperfections on the surface. Regardless of whether the beam is travelled perpendicular to the wafer surface or at an oblique angle for instance 5, 20, 25 to 72 degree, the dark-field collector detects the scattering light from the roughness surface and the imperfections on the surface. Any collected scattering light that above the nominal threshold of light intensity defined as a defect, and then the sizing of defect is defined as a function of defect material (refractive index), its shape (spherical or non-spherical), and a correlated equivalent size with Polystyrene Latex (PSL) spheres of known size deposited on the reference silicon wafer surface [2].

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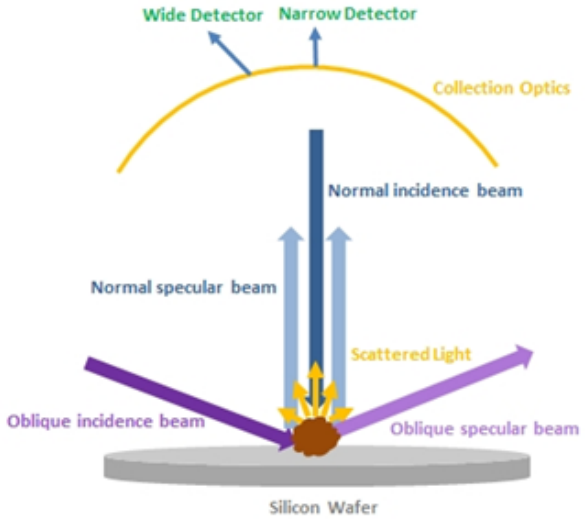

Figure 1. Typical setup of dark-field inspection based on light scattering technology.

Defect classification is one of the most important processes of defect engineering flow and it is also the key focus in this article. Linear-based channeling and rule-based binning are two most effective defect classification algorithms used under the application of light scattering topography. Linear-base Channeling is described statistically as the cross-channel size ratio, which is the function of Dark-field Narrow channel (DN) and Dark-filed Wide channel (DW). The cross-channel size ratio. DN is the captured size of a defect under narrow channel whilst DW is the same defect measured under the wide channel optical path. Using the Linear-based channeling, surface defects are classified into Light Point Defects (LPDs) and Non-cleanable Light Point Defects (LPDNs). A typical ratio n is great than 1 which implies more light scatters will be captured by DN channel collector for LPDNs, in contrast, less light scatters collected by DN channel comparing to DW channel for LPDs. Rule-based binning applies also the concept of cross-channel size ratio but makes the classification process cascaded as to introduce multi-level channeling. Most importantly, it enables positioning (radial or box) feature for predefining Defect of Interest (DOI). This is very useful whilst working together with the crystal originated defect gating using the method of Light Scattering Tomography (LST) [3].

In another study, investigated the hardness and microstructure of components made of 718 alloy. Based on their studies, it was found that heating after forming reduced the hardness of the part by nearly 100%. This is because the low heating temperature causes the transition to the delta phase in the workpiece, which increases the workpiece stiffness. Hihu experimentally formed Haynes 282, alloy 718, alloy 600, SS 316L sheets by a spinning. In this paper, the effect of feed rate was investigated. In addition, we used heating to reduce the hardness of the Haynes and 718 alloys. The results showed that this reduction resulted in the reduction of hardness and improvement of microstructure and hardness of the workpiece and reduction of residual stresses. This paper investigates the spinning of the Hatselloy X alloy to produce a bowl-shaped piece under high thermal stresses. It should be noted that the Hastelloy X alloy loses its plasticity due to its high hardness after cold working. This condition must be attempted to be restored by heating again. In addition, the effect of heating and the effect of microstructures,

hardness of the pieces and their mechanical properties are also investigated.

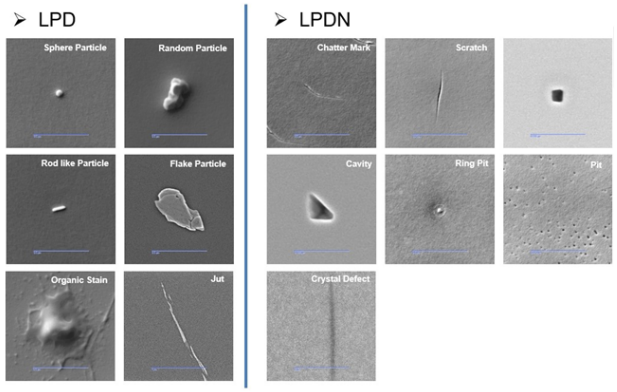

Figure 2. LPD, LPDN high resolution 2D images captured by SEM.

Defect review in particular using Scanning Electron Microscopy (SEM) is the labor intensive and time consuming test method so that it is only suitable as a verification process for the interested defects with the known x-y coordinates on the sample wafer, in addition, it is considered as a destructive method. The process of defect classification and review is often iterative as for optimizing the result of defect classification. The algorithms applied and the parameters set in the recipes of the surface scanning counter must derive from the good understanding of defect origins. Commercially available SEM instrument is used to integrate with Energy Dispersive X-ray spectroscopy (EDX). The x-y coordinates of the captured defects also transfer from the laser scanning counter into SEM-EDX as a saved file. The Localized Light Scatters (LLS) captured by the defect counter (KLA SP5 commercially available) that consists of Light Point Defects (LPDs) such as particles, flakes, residue, stain, sphere and Non-cleanable LPDs (LPDNs) for instance COPs, embedded defects, bump, pit/dent, dimple, scratches, faintline, gouge, will be reviewed by SEM as shown in Figure 2 below. Defect review to identify defects of interest is an effective step for finding root causes in the defect analysis process [4].

Defect analysis includes the activities that using the SEM for defect topographical review, the EDX for elemental analysis of particles, and the root cause finding for the inline manufacturing processes. By identifying the root cause the surface defects, process engineers are able to understand and reduce the PIDs as part of their continuous process improvement activities. Yield enhancement as the objective of defect engineering process is not only from process perspective but also for overall operation roadmap.

Challenges and the goal of defect classification

Using the linear-based channeling with the typical setting of n between 1.1 and 1.3, the surface defects are classified as LPDs and LPDNs. Only if the classification is getting possibly close to the source of defect root cause, which defined as SFPs, COPs, and PIDs, the defect engineers and process engineers are able to measure, analyze and reduce the occurrence of the defects. In reality, as shown in Figure 3, the sectors of A, B and C imply there are always the uncertain sectors based on the linear-based channeling only algorithm. In this article, the approach of combining both linear-based channeling and rule-based binning are applied.

With the proper algorithm tuning, SFPs and COPs can be detected as LPDs and LPDNs separately, the uncertain sector A between SFPs and PIDs and sector B intersects to COPs and PIDs will be reduced if not totally eliminated.

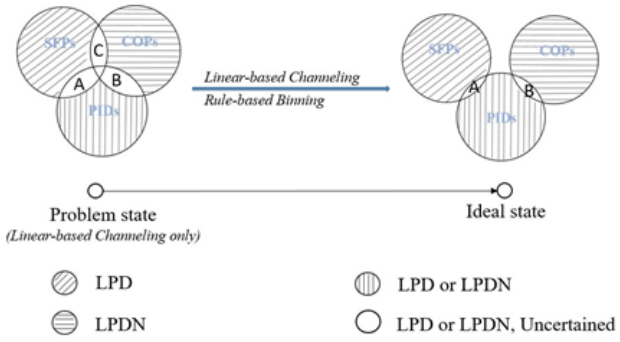

Figure 3. Schematic view of defect classification based linear-based channeling and rule-based binning algorithms: SFPs, COPs and PIDs based on the source of defects; LPDs and LPDNs according to KLA surface scanning counter.

Experiments and Discussion

There are two P type lightly doped silicon mirror polished wafers with the diameter of 300 mm, (100) crystal orientation, thickness at 775 ± 5μm selected for the experiments. Special focus on COPs density and distribution of these two wafers in order to investigate the result of the different algorithms (linear-based channeling and rule-based binning) applied during the process of defect classification: The COP free wafer, which implies the defect type of LPD is dominated as the result of surface scanning counter; KLA SP5 is used in the experiments. This is due to COPs scatters are captured mainly by the DN channel of the optical collector and classified as LPDNs. In this case, the main contributor for the surface defects is PID that is classified as LPDs. The signature pattern of COP wafer with a defect distribution of center disk and ring pattern, which allows defect engineers to apply rule-based binning (radial positioning) for optimizing the purity and accuracy of the defect classification, an Automatic Defect Classification (ADC) process [5].

Choosing the COP free crystal wafers in the experiment, as shown In Fig. 5 the surface defects captured by the surface scanning counter is randomly distributed on the wafer. Most of the LPDs found by SP5 and reviewed by SEM are process induced. There are some SFPs also classified as LPDs correctly. No signature crystal grown-in defect pattern found in terms of defect sizing, density, and distribution. The point defects are distributed in the range of 30 mm to 145 mm cross the radial direction of the wafer. Under this scenario, it is reasonable to apply the algorithm of linear-based channeling in the defect classification process because zero grown-in defects observed with respect to the prime grade of COP free single crystalline silicon. So that, the key focus of the surface defects is Localized Light Scatters (LLS) i.e. the sum of LPDs and LPDs, which is contributed by PIDs and SFPs in the process of silicon wafer manufacturing.

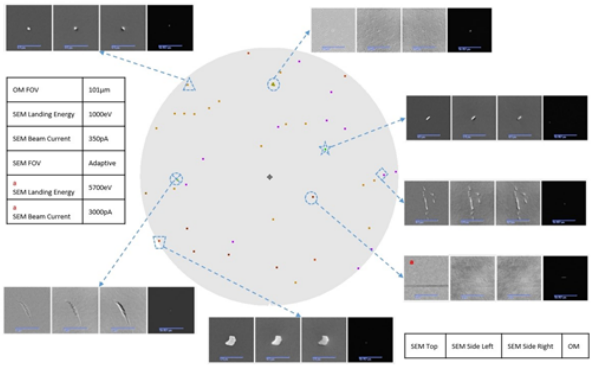

Figure 4. Defect classification using linear-based channeling for COP free single crystal silicon wafer. No specific signature of defect distribution.

In the second experiment, as shown in Figure 4, the silicon wafer with the signature COPs defect distribution (center disk and edge ring pattern) are used. The appearance of varying COPs distribution radially is aligned to the radial dependence of the vacancy concentration. Based on the observation, the COPs are distributed at the central area from 0 to 50 mm, and the edge area of the wafer from 105 mm to 145 mm. Another feature that not shown here is that the high density in the edge areas with the smaller size of COPs (<0.026 μm) comparing to the low density with bigger COPs (>0.032 μm) at the central area of the wafer. With the good understanding of the crystal defects, defect engineers could setup the positioning information of the defects of interest (DOI) according to its radial distribution or box area (2D area) under the classification algorithm of rule-based binning. In this experiment, the defect engineer sets up two areas of DOI, one is the center disk area from the radius o to 50mm and another is the edge ring areas from the radius 105 mm to 145 mm. The defects in these areas are classified as LPDNs by default. Once classified the DOI areas using the positioning feature in the rule-based binning, the defect engineer applied the linear-based channeling as the same as what has been performed in the previous experiment. The PIDs and SFPs will then be captured as LPDs in the exclusion area of DOI if any. In this experiment, there is very less LPDs found based on Detection Limit (DL) of 0.022 μm, which indeed implies the good quality control of fab facilities and inline process.

According to the observations of two special scenarios under the above experiments, both linear-based channeling and rule-based binning algorithms have been verified quantitatively. There could be many other scenarios worth to study under the different products of silicon wafer manufacturing. The objective of the conditional studies is to understand the cases in a simple approach and streamline the troubleshooting process in an effective and efficient manner.

Conclusion

Surface defects response to the several types of device failures in semiconductor manufacturing. An effective defect classification for the surface defects such as COPs, SFPs and PIDs using the commercially available surface scanning counter is needed prior to enhancing product yield and quality. The article demonstrates a novel method of applying linear-based channeling and rule-based binning

algorithms for classifying surface defects on the silicon wafers. The results show that it is fundamental important to understand as-grown crystal defect type, density and size distribution for surface defect metrology as part of the defect engineering.

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