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Predicted Thermal Stress in Flip-Chip and Fine-Pitch-Ball-Grid-Array Designs: Effect of the Underfill Glass Transition Temperature

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Abstract

A previously developed analytical thermal stress model is used for the assessment of the effect of the glass-transition temperature (T_g) of the underfill encapsulant and the thickness of the underfill-solder composite bond (USCB) on the induced stresses. The calculations were carried out for two T_g levels, above and below the operation and testing temperature range for the flip-chip (FC) or the fine-pitch ball-grid-array (FPBGA) assembly with an USCB, and for two thicknesses, 0.05 mm and 0.1 mm, of the USCB. Calculations indicated that the T_g level of the underfill material had a significant effect on the induced stresses: the normal stresses in the USCB with a low-modulus (low T_g) underfill were about half the stresses of the design with high-modulus (high T_g) underfill, and this was true for both thin (0.05 mm thick) and thick (0.1 mm thick) USCB layers. As to the role of the USCB thickness, thicker USCBs exhibit somewhat lower normal stresses, than thin layers, but the effect is insignificant. The maximum predicted shearing stresses occur at the USCB/chip, and not at the USCB/substrate interface. This result is in agreement with the observed, in a number of experiments, delaminations at the USCB/chip interface, and not at the USCB/substrate interface. The obtained data indicate also that (in a way, contrary to the current practice) there is an incentive for using low T_g underfills, provided, of course, that their adhesive strength is proven to be sufficient for the lower stress level. This is an important requirement, of course, and might explain why electronic product manufacturers employ mostly high T_g underfills. As to the incentive for using thicker USCBs, the increase in this thickness from 0.05 mm to 0.1 mm resulted in a minor relief in the normal stress in the USCB for both high and low T_g underfills, but led to an appreciable relief in the interfacial stresses at the USCB/chip interface, especially for high T_g underfills: the predicted stress relief in this case was as significant as 34%. For low Tg underfills the stress relief was much lower, but still appreciable: about 19%. Thicker USCB layers could be more effective, because, as has been shown in our earlier publications and confirmed experimentally, elevated stand-off heights of solder joint interconnections are able to provide appreciable stress relief in the solder material by making the bonding system more compliant. Indeed, for the thickness of 0.75 mm (impossible for FC designs, but rather typical for FPBGA systems) the decrease in the normal stress acting in the USCB cross-sections is appreciable, and the decrease in the shearing stress at the USCB/chip interface is as high as 70% in the case of high T_g underfill and even higher, 76%, in the case of low T_g underfill. The employed analytical stress model used in this analysis can be used for the selection of the adequate underfill material and establishing the appropriate USCB thickness at the design stage. It is noteworthy that, as long as the linear approach is used and the induced stresses are proportional to the change in temperature, the developed model can be used also in situations, when the underfill's T_g is between the temperature extremes that the assembly of interest experiences during its accelerated testing and in actual operation conditions.

Introduction

It has been established that FC and FPBGA package designs is an attractive way to pursue, as far as low-cost and high-reliability of IC packages are concerned. There are, however, situations when the acceptable reliability level in FC and FPBGA technologies cannot be achieved without bringing in surrogate materials, underfills, between the chip and its substrate to strengthen the solder joint interconnections. Underfill technology has been suggested, among other possible encapsulation technologies, about three decades ago [1], but has become the technology of choice in the today's IC packaging [2-12]. Solder material fatigue failures because of the inelastic strains in the peripheral portions of the solder joint interconnections and delaminations (typically at the chip-solder interface) were observed as the main failure modes in FC and FPBGA structures with underfills [13-27]. It is expected that the appropriately chosen underfill material and the adequate application technology will improve the situation. First of all, one should determine if it would be possible to get away with an un-encapsulated design ("to underfill or not to underfill?") and still meet the reliability requirements. If an underfill decision is made, one should select the adequate underfill material and technology, with consideration of numerous factors associated with the application of this technology: encapsulation process, time-to-market (completion), cost, manufacturability, testability, reparability, etc.

Some existing experiments show that 1) packages with high-T_g underfills are less sensitive to the 85°C/85%RH temperature-humidity bias, that 2) high T_g underfills lead to somewhat higher induced curvatures than low T_g underfills, that 3) packages with low-T_g underfills exhibit during cooling processes appreciable stress relaxation; that 4) the final deformations of the packages (this takes place at low temperature

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conditions, when the difference in the thermal strains between the chip and its substrate is the highest) depend, in low T_g underfills, also on the cooling rate, and that 5) the underfill behavior depends not only on the T_g level, but also on the width of the T_g region and its slope. Zhang Z et al. conclude that "as long as the accurate temperature-dependent properties of underfill are not used, the predicted solder fatigue life based on a single value of T_g and a sharp transition is subject to skepticism" and that the "lifetime variation can be 80% less for steeper slope and doubled for a shallower slope". This means particularly that the "steep slope" assumption is conservative: it results in a somewhat shorter predicted fatigue life.

In the analysis that follows the role of one important characteristic of the USCB is addressed: the glass transition temperature (T_g) of the underfill epoxy [28-30]. Below T_g the epoxy is in a hard (glassy) state. Above the T_g it transitions to a rubbery state and, as a result, the material's modulus decreases and its CTE increases. There is also an indication that, for many epoxies, their cohesive and adhesive strength is lower above the T_g. The latter drawback might be, however, a lesser problem, considering that the applications of a low T_g epoxy might lead to considerably lower stresses. In the analysis carried out in the current paper it is shown that this might be indeed the case. The role of the USCB thickness is also assessed. The stresses considered in this analysis include normal stresses acting in the cross-sections of the chip, the substrate, and the USCB, and the shearing stresses at the USCB interfaces with the chip and the substrate. Since the USCB bonding layer is comprised of a relatively high-modulus solder and low-modulus epoxy underfill (even when the underfill epoxy is loaded with fillers), and is characterized therefore, unlike in adhesively bonded joints, by a relatively high effective Young's modulus, a tri- and not a bi-material predictive model [31-33] is employed.

Analysis

Assumptions

The following major assumptions were used in this analysis:

• Structural analysis (strength-of-materials) approach can be applied to evaluate the induced stresses, so that no singular stresses can possibly occur at the assembly edges. From the theory-of-elasticity standpoint, the predicted stresses can be viewed as useful design-for-reliability parameters that characterize the state of stress in the bonded assembly of interest, including its edge portions.

• The assembly and its constituents (components) can be treated as thin elongated plates, experiencing small deflections. The engineering theory of such plates can be employed therefore to determine the stresses and the deflections.

• The interfacial shearing stresses and the total assembly curvature can be evaluated without considering the effect of the peeling stresses – normal interfacial stresses acting in the through-thickness direction of the assembly. The peeling stresses, which are proportional to the longitudinal gradient of the interfacial shearing stresses, can be then determined, if necessary, from the evaluated shearing stresses.

• The shearing stresses can be found, based on the concept of the interfacial compliance [34], assuming that the interfacial displacements of the assembly components can be represented as a sum of unrestricted (stress-free) thermal displacements; displacements, predicted using Hooke's law and calculated under an assumption that these displacements are the same for the entire cross-section of the given assembly component; and corrections considering that, in reality, the interfacial displacements are somewhat larger than the displacements of the inner points of the given cross-section. In addition, it is assumed that these corrections are proportional to the interfacial shearing stress in the given cross-section and are not affected by the stresses and strains in the adjacent cross-sections;

• The effect of the assembly bow is not considered in this analysis;

• The dependence of the mechanical properties (Young's modulus and CTE) of the underfill material of temperature is a step-wise function; in other words, the glass-transition temperature T_g is characterized by a single number; based on the Zhang Z information, it is a conservative assumption.

Thermally induced forces and interfacial stresses

The following formulas can be used for the evaluation of the thermally induced forces and the interfacial shearing stresses [33]:

1. Thermally induced forces in the mid-portion of a long flip-chip/substrate assembly:

$$T_1 = \frac{(\alpha_1-\alpha_2)\lambda_0+(\alpha_1-\alpha_0)\lambda_2}{\lambda_0\lambda_1+\lambda_1\lambda_2+\lambda_2\lambda_0}\Delta t,\quad T_1 = \frac{(\alpha_1-\alpha_2)\lambda_0+(\alpha_1-\alpha_0)\lambda_2}{\lambda_0\lambda_1+\lambda_1\lambda_2+\lambda_2\lambda_0}\Delta t,$$

$$T_2 = \frac{(\alpha_2-\alpha_1)\lambda_0+(\alpha_2-\alpha_0)\lambda_1}{\lambda_0\lambda_1+\lambda_1\lambda_2+\lambda_2\lambda_0}\Delta t \qquad (1)$$

Here T_1 is the change in temperature from the elevated (manufacturing) temperature to the low (room, testing, operation, T_g) temperature; T_0, T_1 and T_2 are the thermally induced forces (per unite assembly width) acting in the mid-portion of the (underfilled) solder layer (zero component), the chip (component #1), and in the substrate (component #2), respectively; α_0, α_1 and α_2 are the effective CTE's of the materials; $\lambda_i = \frac{1-\nu_i}{E_i h_i}, i=0,1,2$ are the effective axial compliances of the assembly components; $E_i, i=0,1,2$, are the effective Young's moduli of the materials; $\nu_i, i=0,1,2$, are their Poisson's ratios; and $h_i, i=0,1,2$ are the assembly component thicknesses.

2. Distributed thermally induced forces:

$$T_0(x) = T_0\left(1-\frac{\cosh kx}{\cosh kl}\right),\quad T_1(x) = T_1\left(1-\frac{\cosh kx}{\cosh kl}\right),\quad T_2(x) = T_2\left(1-\frac{\cosh kx}{\cosh kl}\right) \qquad (2)$$

Here k is half the assembly length, and k is the thus far unknown parameter of the assembly. Here

$$k = \sqrt{\frac{k_1^2+k_2^2}{2}\left[1+\sqrt{1-\delta\left(\frac{2k_1k_2}{k_1^2+k_2^2}\right)^2}\right]} \qquad (3)$$

is the parameter of the interfacial shearing stress,

$$k_1 = \sqrt{\frac{\lambda_0+\lambda_1}{\kappa_0+\kappa_1}},\quad k_2 = \sqrt{\frac{\lambda_0+\lambda_2}{\kappa_0+\kappa_2}}, \qquad (4)$$

are the "partial" parameters of the interfacial shearing stresses,

$$\delta = \frac{\lambda_0\lambda_1+\lambda_1\lambda_2+\lambda_2\lambda_0}{(\lambda_0+\lambda_1)(\lambda_0+\lambda_2)} \qquad (5)$$

is the factor of the axial compliances of the assembly components, $\kappa_0 = \frac{h_0}{G_0}$ is the longitudinal interfacial compliance of the solder layer; G_0 is the effective shear modulus of this layer; $\kappa_i = \frac{h_i}{3G_i}, i=1,2$ are the longitudinal interfacial compliances of the chip and the substrate, respectively; $G_i = \frac{E_i}{2(1+\nu_i)}, i=0,1,2$ are the shear moduli of the components' materials.

3. Interfacial shearing stresses:

$$\tau_1(x) = \frac{dT_1(x)}{dx} = -kT_1 \frac{\sinh kx}{\cosh kl}, \quad \tau_2(x) = \frac{dT_2(x)}{dx} = -kT_2 \frac{\sinh kx}{\cosh kl} \qquad (6)$$

The signs of these stresses depend on the signs of the forces T_1 and T_2, and the signs of these forces, whether tensile (+) or compressive (-), are determined by the formulas (1).

The highest shearing stresses take place, in accordance with this model, at the end cross-sections:

$$\tau_1(l) = -kT_1 \tanh kl, \quad \tau_2(l) = -kT_2 \tanh kl. \qquad (7)$$

For $kl \succ 2.5$ these stresses become assembly size independent:

$$\tau_1(l) = -kT_1, \quad \tau_2(l) = -kT_2. \qquad (8)$$

Computed Data

Computed Data is shown in the below Tables 1-7.

Component # Properties	0 (Underfilled solder)	1 (Chip)	2 (Substrate)
Effective CTE, α, $1/{}^0C$	$60x10^{-6}$	$2.2x10^{-6}$	$13.2x10^{-6}$
Effective Young's modulus, $E, kg/mm^2$	2000	12300	2000
Poisson's ratio, *V*	0.40	0.24	0.30
Shear modulus $G = \frac{E}{2(1+v)}, kg/mm^2$	714.3	4959.7	769.2
Thickness, *h,m*	0.05	0.5	1.5
Axial compliance $\lambda = \frac{1-v}{Eh}, mm/kg$	$60.0000x10^{-4}$	$1.2358x10^{-4}$	$2.3333x10^{-4}$
Axial compliance factor $F = \lambda_0\lambda_1 + \lambda_1\lambda_2 + \lambda_2\lambda_0, mm^2/kg^2$	$217.0295x10^{-8}$		
Thermal forces, kg/mm $T_0 = \frac{\Delta t}{F}[(\alpha_0-\alpha_1)\lambda_2 + (\alpha_0-\alpha_2)\lambda_1],$ $T_1 = \frac{\Delta t}{F}[(\alpha_1-\alpha_2)\lambda_0 + (\alpha_1-\alpha_0)\lambda_2],$ $T_2 = \frac{\Delta t}{F}[(\alpha_2-\alpha_1)\lambda_0 + (\alpha_2-\alpha_0)\lambda_1].$	150.3194	-620.0493	469.7299
Normal stresses $\sigma = \frac{T}{h}, kg/mm^2$	3006.3880	-1240.0986	313.1533
Interfacial compliance, κ, $\kappa_0 = \frac{h_0}{G_0}, \kappa_1 = \frac{h_1}{3G_1}, \kappa_2 = \frac{h_2}{3G_2}. mm^3/kg$	$0.7000x10^{-4}$	$0.3360x10^{-4}$	$6.5003x10^{-4}$
Factor of the relative axial compliance $\delta = \frac{F}{(\lambda_0+\lambda_1)(\lambda_0+\lambda_2)}$	0.056858		
Chip-to-solder parameter of the interfacial shearing stress $k_1 = \sqrt{\frac{\lambda_0+\lambda_1}{\kappa_0+\kappa_1}}, mm^{-1}$		7.6882	
Substrate-to-solder parameter of the interfacial shearing stress $k_2 = \sqrt{\frac{\lambda_0+\lambda_2}{\kappa_0+\kappa_2}}, mm^{-1}$			2.9423
Parameter of the interfacial shearing stress $k = \sqrt{\frac{k_1^2+k_2^2}{2}\left[1+\sqrt{1-\delta\left(\frac{2k_1k_2}{k_1^2+k_2^2}\right)^2}\right]}, mm^{-1}.$	8.2057		
Shearing stress at chip-solder interface $\tau_1(l) = -kT_1, kg/mm^2$		5087.9305	
Shearing stress at solder-PCB interface $\tau_2(l) = -kT_2, kg/mm^2$			-3854.4626
Curing temperature 150^0C; low temperature 170^0C; Change in temperature 170^0C;			

Table 1: High T_g (above the curing temperature), high modulus, low expansion and 0.05mm thick underfill.

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Component # Properties	0 (Underfilled solder)	1 (Chip)	2 (Substrate)
Effective CTE, α, $1/^0C$	$120x10^{-6}$	$2.2x10^{-6}$	$13.2x10^{-6}$
Effective Young's modulus, $E, kg/mm^2$	400	12300	2000
Effective Poisson's ratio, ν	0.45	0.24	0.30
Shear modulus $G = \frac{E}{2(1+\nu)}, kg/mm^2$	137.9310	4959.7	769.3
Thickness, h, mm	0.05	0.5	1.5
Axial compliance $\lambda = \frac{1-\nu}{Eh}, mm/kg$	$275x10^{-4}$	$1.2358x10^{-4}$	$2.3334x10^{-4}$
Axial compliance factor $F = \lambda_0\lambda_1 + \lambda_1\lambda_2 + \lambda_2\lambda_0, mm^2/kg^2$	$984.4136x10^{-8}$		
Thermal forces, kg/mm $T_0 = \frac{\Delta t}{F}[(\alpha_0 - \alpha_1)\lambda_2 + (\alpha_0 - \alpha_2)\lambda_1],$ $T_1 = \frac{\Delta t}{F}[(\alpha_1 - \alpha_2)\lambda_0 + (\alpha_1 - \alpha_0)\lambda_2],$ $T_2 = \frac{\Delta t}{F}[(\alpha_2 - \alpha_1)\lambda_0 + (\alpha_2 - \alpha_0)\lambda_1].$	70.2611	-569.8619	499.6008
Normal stress $\sigma = \frac{T}{h}, kg/mm^2$	1405.2220	-1139.7238	333.0672
Interfacial compliance of the components, κ, $\kappa_0 = \frac{h_0}{G_0}, \kappa_1 = \frac{h_1}{3G_1}, \kappa_2 = \frac{h_2}{3G_{20}}. mm^3/kg$	$3.6250x10^{-4}$	$0.3360x10^{-4}$	$6.4994x10^{-4}$
Factor of the axial compliance $\delta = \frac{F}{(\lambda_0 + \lambda_1)(\lambda_0 + \lambda_2)}$	0.012850		
Partial (chip-to-solder) parameter of the interfacial shearing stress $k_1 = \sqrt{\frac{\lambda_0 + \lambda_1}{\kappa_0 + \kappa_1}}, mm^{-1}$		5.5931	
Partial (substrate-to-solder) parameter of the interfacial shearing stress $k_2 = \sqrt{\frac{\lambda_0 + \lambda_2}{\kappa_0 + \kappa_2}}, mm^{-1}$			3.2995
Parameter of the interfacial shearing stress $k = \sqrt{\frac{k_1^2 + k_2^2}{2}\left[1 + \sqrt{1 - \delta\left(\frac{2k_1k_2}{k_1^2 + k_2^2}\right)^2}\right]}, mm^{-1}.$	9.8427		
Shearing stress at chip-solder interface $\tau_1(l) = -kT_1, kg/mm^2$		4061.7032	
Shearing stress at solder-PCB interface $\tau_2(l) = -kT_2, kg/mm^2$			-3035.8392
Curing temperature is 150^0C; low temperature is 170^0C; Change in temperature from the curing temperature to the low temperature is therefore 170^0C;			

Table 2: Low T_g (below the lowest temperature possible), low modulus, high expansion and 0.05 mm thick underfill.

Conclusions and Future Work

The following conclusions can be drawn from the calculated data:

- The maximum predicted shearing stresses occur indeed at the USCB/chip, and not at the USCB/substrate interface, and this result is in agreement with the observed delaminations at the USCB/chip interface.
- The calculated data indicate that there is an incentive for using low T_g underfills, provided, of course, that their adhesive strength is proven to be sufficient. This might me less of a challenge, even if the cohesive and the adhesive strength of the USCB layer with a low T_g is not very high, but the applied stresses are also relatively low.
- As to the incentive for using thicker USCBs, the increase in this thickness from 0.05 mm to 0.1 mm resulted in rather minor relief

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Component # Properties	0 (Underfilled solder)	1 (Chip)	2 (Substrate)
Effective CTE, α, $1/^0C$	$60x10^{-6}$	$2.2x10^{-6}$	$13.2x10^{-6}$
Effective Young's modulus, $E, kg/mm^2$	2000	12300	2000
Poisson's ratio, ν	0.40	0.24	0.30
Shear modulus $G=\frac{E}{2(1+\nu)}, kg/mm^2$	714.3	4959.7	769.2
Thickness, h, mm	0.1	0.5	1.5
Axial compliance $\lambda=\frac{1-\nu}{Eh}, mm/kg$	$30.0000x10^{-4}$	$1.2358x10^{-4}$	$2.3333x10^{-4}$
Axial compliance factor $F=\lambda_0\lambda_1+\lambda_1\lambda_2+\lambda_2\lambda_0, mm^2/kg^2$	$109.9595x10^{-8}$		
Thermal forces, kg/mm $T_0=\frac{\Delta t}{F}[(\alpha_0-\alpha_1)\lambda_2+(\alpha_0-\alpha_2)\lambda_1]$, $T_1=\frac{\Delta t}{F}[(\alpha_1-\alpha_2)\lambda_0+(\alpha_1-\alpha_0)\lambda_2]$, $T_2=\frac{\Delta t}{F}[(\alpha_2-\alpha_1)\lambda_0+(\alpha_2-\alpha_0)\lambda_1]$.	297.9190	-718.6920	420.7730
Normal stress $\sigma=\frac{T}{h}, kg/mm^2$	2979.1900	-1437.3840	280.5153
Interfacial compliance, κ, $\kappa_0=\frac{h_0}{G_0}$, $\kappa_1=\frac{h_1}{3G_1}$, $\kappa_2=\frac{h_2}{3G_2}$. mm^3/kg	$1.4000x10^{-4}$	$0.3360x10^{-4}$	$6.5003x10^{-4}$
Factor of the relative axial compliance $\delta=\frac{F}{(\lambda_0+\lambda_1)(\lambda_0+\lambda_2)}$		0.108875	
Chip-to-solder parameter of the interfacial shearing stress $k_1=\sqrt{\frac{\lambda_0+\lambda_1}{\kappa_0+\kappa_1}}, mm^{-1}$		4.2418	
Substrate-to-solder parameter of the interfacial shearing stress $k_2=\sqrt{\frac{\lambda_0+\lambda_2}{\kappa_0+\kappa_2}}, mm^{-1}$			2.0230
Parameter of the interfacial shearing stress $k=\sqrt{\frac{k_1^2+k_2^2}{2}\left[1+\sqrt{1-\delta\left(\frac{2k_1k_2}{k_1^2+k_2^2}\right)^2}\right]}, mm^{-1}$.		4.6601	
Shearing stress at chip-solder interface $\tau_1(l)=-kT_1, kg/mm^2$		3349.1683	
Shearing stress at solder-PCB interface $\tau_2(l)=-kT_2, kg/mm^2$			-1960.8443
Curing temperature 150^0C; low temperature -20^0C; Change in temperature 170^0C;			

Table 3: High T_g (above the curing temperature), high modulus, low expansion and 0.1mm thick underfill

in the normal stress in the bond for both high and low T_g underfills, but led to an appreciable relief in the interfacial stresses at the USCB/chip interface, especially for high T_g underfills. The stress relief for them was as high as 34%. For low T_g underfills the relief was much lower, about 19%. However, for the thickness of 0.75 mm (impossible for FC designs, but quite typical for FPBGA systems) the decrease in the normal stress

Component # Properties	0 (Underfilled solder)	1 (Chip)	2 (Substrate)
Effective CTE, α, $1/^0C$	$60x10^{-6}$	$2.2x10^{-6}$	$13.2x10^{-6}$
Effective Young's modulus, $E, kg/mm^2$	400	12300	2000
Effective Poisson's ratio, ν	0.45	0.24	0.30
Shear modulus $G=\frac{E}{2(1+\nu)}, kg/mm^2$	137.9310	4959.7	769.3
Thickness, h, mm	0.1	0.5	1.5
Axial compliance $\lambda=\frac{1-\nu}{Eh}, mm/kg$	$137.5x10^{-4}$	$1.2358x10^{-4}$	$2.3334x10^{-4}$
Axial compliance factor $F=\lambda_0\lambda_1+\lambda_1\lambda_2+\lambda_2\lambda_0$, mm^2/kg^2	$493.6486x10^{-8}$		
Thermal forces, kg/mm $T_0=\frac{\Delta t}{F}[(\alpha_0-\alpha_1)\lambda_2+(\alpha_0-\alpha_2)\lambda_1],$ $T_1=\frac{\Delta t}{F}[(\alpha_1-\alpha_2)\lambda_0+(\alpha_1-\alpha_0)\lambda_2],$ $T_2=\frac{\Delta t}{F}[(\alpha_2-\alpha_1)\lambda_0+(\alpha_2-\alpha_0)\lambda_1].$	140.1369	-615.6379	475.5010
Normal stress $\sigma=\frac{T}{h}, kg/mm^2$	1401.3690	-1231.2758	317.0007
Interfacial compliance of the components, κ, $\kappa_1=\frac{h_1}{3G_1}$, $\kappa_1=\frac{h_1}{3G_1}$, $\kappa_2=\frac{h_2}{3G_2}$. mm^3/kg	$7.2500x10^{-4}$	$0.3360x10^{-4}$	$6.4994x10^{-4}$
Factor of the axial compliance $\delta=\frac{F}{(\lambda_0+\lambda_1)(\lambda_0+\lambda_2)}$	0.025446		
Partial (chip-to-solder) parameter of the interfacial shearing stress $k_1=\sqrt{\frac{\lambda_0+\lambda_1}{\kappa_0+\kappa_1}}, mm^{-1}$		4.2765	
Partial (substrate-to-solder) parameter of the interfacial shearing stress $k_2=\sqrt{\frac{\lambda_0+\lambda_2}{\kappa_0+\kappa_2}}, mm^{-1}$			3.1891
Parameter of the interfacial shearing stress $k=\sqrt{\frac{k_1^2+k_2^2}{2}\left[1+\sqrt{1-\delta\left(\frac{2k_1k_2}{k_1^2+k_2^2}\right)^2}\right]}, mm^{-1}.$	5.3190		
Shearing stress at chip-solder interface $\tau_1(l)=-kT_1, kg/mm^2$		3274.5560	
Shearing stress at solder-PCB interface $\tau_2(l)=-kT_2, kg/mm^2$			-2529.1898
Curing temperature is 150^0C; low temperature is -20^0C; Change in temperature from the curing temperature to the low temperature is therefore 170^0C;			

Table 4: Low T_g (below the lowest temperature possible), low modulus, high expansion and 0.1mm thick underfill.

Component # Properties	0 (Underfilled solder)	1 (Chip)	2 (Substrate)
Effective CTE, α, $1/{}^0C$	$60x10^{-6}$	$2.2x10^{-6}$	$13.2x10^{-6}$
Effective Young's modulus, $E, kg/mm^2$	2000	12300	2000
Poisson's ratio, ν	0.40	0.24	0.30
Shear modulus $G = \frac{E}{2(1+\nu)}, kg/mm^2$	714.3	4959.7	769.2
Thickness, h, mm	0.75	0.5	1.5
Axial compliance $\lambda = \frac{1-\nu}{Eh}, mm/kg$	$4.0000x10^{-4}$	$1.2358x10^{-4}$	$2.3333x10^{-4}$
Axial compliance factor $F = \lambda_0\lambda_1 + \lambda_1\lambda_2 + \lambda_2\lambda_0, mm^2/kg^2$	$17.1604x10^{-8}$		
Thermal forces, kg/mm $T_0 = \frac{\Delta t}{F}[(\alpha_0-\alpha_1)\lambda_2 + (\alpha_0-\alpha_2)\lambda_1]$, $T_1 = \frac{\Delta t}{F}[(\alpha_1-\alpha_2)\lambda_0 + (\alpha_1-\alpha_0)\lambda_2]$, $T_2 = \frac{\Delta t}{F}[(\alpha_2-\alpha_1)\lambda_0 + (\alpha_2-\alpha_0)\lambda_1]$.	1909.0414	-1771.9806	-137.0608
Normal stress $\sigma = \frac{T}{h}, kg/mm^2$	2545.3885	-3543.9612	-91.3739
Interfacial compliance, κ, $\kappa_0 = \frac{h_0}{G_0}$, $\kappa_1 = \frac{h_1}{3G_1}$, $\kappa_2 = \frac{h_2}{3G_2}$. mm^3/kg	$10.4998x10^{-4}$	$0.3360x10^{-4}$	$6.5003x10^{-4}$
Factor of the relative axial compliance $\delta = \frac{F}{(\lambda_0+\lambda_1)(\lambda_0+\lambda_2)}$	0.517496		
Chip-to-solder parameter of the interfacial shearing stress $k_1 = \sqrt{\frac{\lambda_0+\lambda_1}{\kappa_0+\kappa_1}}, mm^{-1}$		0.6951	
Substrate-to-solder parameter of the interfacial shearing stress $k_2 = \sqrt{\frac{\lambda_0+\lambda_2}{\kappa_0+\kappa_2}}, mm^{-1}$			0.6104
Parameter of the interfacial shearing stress $k = \sqrt{\frac{k_1^2+k_2^2}{2}\left[1+\sqrt{1-\delta\left(\frac{2k_1k_2}{k_1^2+k_2^2}\right)^2}\right]}, mm^{-1}$.	0.8531		
Shearing stress at chip-solder interface $\tau_1(l) = -kT_1, kg/mm^2$		1511.6946	
Shearing stress at solder-PCB interface $\tau_2(l) = -kT_2, kg/mm^2$			-116.9266
Curing temperature 150^0C; low temperature -20^0C; Change in temperature 170^0C;			

Table 5: High T_g (above the curing temperature), high modulus, low expansion and 0.75 mm thick underfill.

Component # Properties	0 (Underfilled solder)	1 (Chip)	2 (Substrate)
Effective CTE, α, $1/^0C$	$120x10^{-6}$	$2.2x10^{-6}$	$13.2x10^{-6}$
Effective Young's modulus, $E, kg/mm^2$	400	12300	2000
Effective Poisson's ratio, ν	0.45	0.24	0.30
Shear modulus $G=\frac{E}{2(1+\nu)}, kg/mm^2$	137.9310	4959.7	769.3
Thickness, h, mm	0.75	0.5	1.5
Axial compliance $\lambda=\frac{1-\nu}{Eh}, mm/kg$	$18.3333x10^{-4}$	$1.2358x10^{-4}$	$2.3334x10^{-4}$
Axial compliance factor $F=\lambda_0\lambda_1+\lambda_1\lambda_2+\lambda_2\lambda_0, mm^2/kg^2$	$68.3188x10^{-8}$		
Thermal forces, kg/mm $T_0=\frac{\Delta t}{F}[(\alpha_0-\alpha_1)\lambda_2+(\alpha_0-\alpha_2)\lambda_1],$ $T_1=\frac{\Delta t}{F}[(\alpha_1-\alpha_2)\lambda_0+(\alpha_1-\alpha_0)\lambda_2],$ $T_2=\frac{\Delta t}{F}[(\alpha_2-\alpha_1)\lambda_0+(\alpha_2-\alpha_0)\lambda_1].$	1012.3846	-1185.7792	173.3947
Normal stress $\sigma=\frac{T}{h}, kg/mm^2$	1349.8461	-2371.5584	115.5965
Interfacial compliance of the components, κ, $\kappa_0=\frac{h_0}{G_0}, \kappa_1=\frac{h_1}{3G_1}, \kappa_2=\frac{h_2}{3G_{20}} \cdot mm^3/kg$	$54.3750x10^{-4}$	$0.3360x10^{-4}$	$6.4994x10^{-4}$
Factor of the axial compliance $\delta=\frac{F}{(\lambda_0+\lambda_1)(\lambda_0+\lambda_2)}$	0.168927		
Partial (chip-to-solder) parameter of the interfacial shearing stress $k_1=\sqrt{\frac{\lambda_0+\lambda_1}{\kappa_0+\kappa_1}}, mm^{-1}$		0.5981	
Partial (substrate-to-solder) parameter of the interfacial shearing stress $k_2=\sqrt{\frac{\lambda_0+\lambda_2}{\kappa_0+\kappa_2}}, mm^{-1}$			0.5827
Parameter of the interfacial shearing stress $k=\sqrt{\frac{k_1^2+k_2^2}{2}\left[1+\sqrt{1-\delta\left(\frac{2k_1k_2}{k_1^2+k_2^2}\right)^2}\right]}, mm^{-1}.$	0.8163		
Shearing stress at chip-solder interface $\tau_1(l)=-kT_1, kg/mm^2$		967.9516	
Shearing stress at solder-PCB interface $\tau_2(l)=-kT_2, kg/mm^2$			-141.5421
Curing temperature is 170^0C; low temperature is 170^0C; Change in temperature from the curing temperature to the low temperature is therefore 170^0C;			

Table 6: Low T_g (below the lowest temperature possible), low modulus, high expansion and 0.75mm thick underfill.

Stress, kg/mm^2		**0.05 mm thick underfill**		**0.10 mm thick underfill**		**0.75 mm thick underfill**	
		High T_g	Low T_g	High T_g	Low T_g	High T_g	Low T_g
Normal stress	in the underfill σ_0	3006	1405	2979	1401	2545	1350
	in the chip σ_1	-1240	-1140	-1437	-1231	-3544	-2372
	in the substrate τ_1	313	333	280	317	-91	116
Shearing stress	at the underfill-chip interface τ_1	5088	4062	3349	3275	1512	968
	at the underfill-substrate interface τ_2	-3854	-3036	-1961	-2529	-117	-141

Table 7: Calculated stresses.

in the bond is appreciable, and the decrease in the shearing stress at the USCB with the chip is as high as 70% in the case of high T_g underfill and 76% in the case of low T_g underfill.

- Thicker USCB layers could be more affective, because, as has been shown earlier, elevated stand-off heights of solder joint interconnections are able to provide appreciable stress relief in the solder joints by making the bond more compliant. This should be attributed in part to the use of solder joints with elevated stand-off heights [35].

Future work should include

- FEA evaluations and experimental verification of the obtained information,
- Development of a predictive model for the case when the T_g of the underfill is between the curing and the low temperatures, and for the situation when the dependences of the Young's modulus and CTE of the underfill are characterized by a non-zero width of the transition region; in effect, the developed model can be used for that;
- Methodology for the evaluation of the role of the visco-elastic behavior of the underfill material;
- Methodology for the evaluation of the effective modulus and CTE of the USCB layer [35].

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References

1. Suhir E, Segelken JM (1990) Mechanical behavior of flip-chip encapsulants. J Electr Packaging 112: 327-332.
2. Lau J, Powers-Maloney LM, Baker JR, Rice D, Shaw B (1989) Solder joint reliability of fine pitch surface mount technology assemblies. 7-th IEEE/CHMT Int Electronic Manufacturing Technology Symp San Francisco, CA, USA.
3. Chai K, Wu E, Hsieh R, Tong JY (2002) Challenge of flip chip encapsulation technologies. Proceedings of SPIE, Denver, CO, USA.
4. Ghaffarian R (2012) Underfill Optimization for FPGA Package/Assembly. Jet Propulsion Lab, Pasadena, CA, USA.
5. Suryanarayana D, Hsiao R, Gall TP, McCreary JM (1991) Enhancement of flip-chip fatigue life by encapsulation. IEEE Trans Compon Hybrids Manuf Tech 14: 218-223.
6. Suryanarayana D, Wu TY, Varcoe JA (1993) Encapsulants used in flip-chip packages. 43rd ECTC, Orlando, FL, USA.
7. Clementi J, McCreary J, Niu TM, Palomaki J, Varcoe J, et al. (1993) Flip chip encapsulation on ceramic substrates. IEEE 43rd ECTC, Orlando, FL, USA.
8. Lau JH (1995) Flip Chip Technologies. McGraw-Hill: New York, NY, USA.
9. Wong CP, Lou S, Zhang Z (2000) Flip-the-chip. Science 290: 2269-2270.
10. Lau JH, Chang C (1999) How to select underfill materials for solder bumped flip-chips on low cost substrates? Int J Microcircuits Electron.
11. Nysaether JB, Lundstrom P, Liu J (1997) Measurements of solder bumps lifetime as a function of the underfill material properties. 1-st IEEE Int. Symp on Polymeric Electronics Packaging, PEP '97.
12. Chen T, Wang J, Lu D (2004) Emerging challenges of underfill for flip-chip applications. 54th ECTC, Las Vegas, NV, USA.
13. Semmens JE, Adams T (1998) Flip chip package failure mechanism. Solid State Technol.
14. Dudek R, Schubert A, Michel B (2000) Analysis of flip chip attach reliability. 4th Int. Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing, Espoo, Finland.
15. Mercado L, Sarihan V (2003) Evaluation of the die attach cracking in flip-chip PBGA packages. IEEE CPMT Trans 2: 719-723.
16. Hirohata K, Kawamura N, Mukai M, Kawakami T, Aoki H, et al. (2002) Mechanical fatigue test method for chip/underfill delamination in flip-chip packages. IEEE Trans Electron Packag Manuf 25: 217-222.
17. Fan XJ, Wang HB, Lim TB (2001) Investigation of the underfill delamination and cracking in flip-chip modules under temperature cyclic loading. IEEE Trans Compon Packag Tech.
18. Zhai CJ, Blish RC, Master RN (2004) Investigation and minimization of underfill delamination in flip chip packages. IEEE Trans Dev Mater Reliabil 4: 86-91.
19. Kwak JB, Chung S (2012) The effects of underfill on the thermal fatigue reliability of solder joints in newly developed flip chip on module. IEEE I-Therm, San Diego, CA, USA.
20. Rzepka S, Korhonen M, Meusel E, Li CY (1998) The effect of underfill and underfill delamination on the thermal stress in flip-chip solder joints. J Electron Packag 120: 342-348.
21. Su P, Rzepka S, Korhonen M (1999) The effects of underfill on the reliability of flip chip solder joints. J Electron Mater 28: 1017-1022.
22. Lau J, Lee S, Chang C, Ouyang C (2000) Effects of underfill material properties on the reliability of solder bumped flip chip on board with imperfect underfill encapsulants. IEEE CPMT Transactions 23: 323-333.
23. Dutta I, Gopinath A, Marshall C (2002) Underfill constraint effects during thermo-mechanical cycling of flip-chip solder joints. J Electron Mater 31: 253-264.
24. Wang T, Lai Y, Wu J (2003) Effect of underfill thermo-mechanical properties on thermal cycling fatigue reliability of flip-chip ball grid array. J Electron Packag 126: 560-564.
25. Kuo CT, Yip MC, Chiang KN (2004) Time and temperature-dependent mechanical behavior of underfill materials in electronic packaging application. Microelectronics Reliability 44: 627-638.
26. Noh BI, Lee BY, Jung SB (2008) Thermal fatigue performance of SnAgCu chip-scale package with underfill. Mater Sci Eng A Struct Mater 483: 464-468.
27. Tsai MY, Lin YC, Huang CY, Wu JD (2005) Thermal deformations and

stresses of flip-chip BGA packages with low- and high-Tg underfills. IEEE Trans Electron Packag Manuf 28: 328-337.

28. Chang JY, Huang SSSY, Lee CC, Chuang TC (2015) Influence of glass transition temperature of underfill on the stress behavior and reliability of microjoints within a chip stacking architecture. ASME J Electron Packag.

29. Zhang Z, Park SB, Darbha K, Master RN (2010) Effect of glass transition slope of underfill on solder joint fatigue life. 11th Int. Conference on Electronic Packaging Technology & High Density Packaging.

30. Suhir E (2017) Flip-chip assembly: is a bi-material model acceptable? J Materials in Electronics 28: 15775-15781.

31. Suhir E (2018) Analytical thermal stress model for a typical flip-chip package design. J Mater Sci Materials in Electronics 29: 2676-2688.

32. Suhir E (2001) Analysis of interfacial thermal stresses in a tri-material assembly. J Appl Phys 89: 3685-3694.

33. Suhir E (1986) Stresses in bi-metal thermostats. ASME J Appl Mech 53: 657-660.

34. Suhir E (2015) Analysis of a short beam with application to solder joints: could larger stand-off heights relieve stress? Eur J Appl Phys.

35. Qu J, Wong CP (2002) Effective elastic modulus of underfill material for flip-chip applications. IEEE CPMT Trans 25: 53-55.