Mini Review
Volume 11:08, 2022

Journal of Electrical & Electronic Systems

ISSN: 2332-0796 Open Access

Photonic Integrated Heterogeneous 2 Dimensional/3 Dimensional Microsystems

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Abstract

The requirement for large-scale heterogeneous integration is being driven by the ongoing trend of exponential development in data communications and processing. We are seeing an increasing tendency in the development of 3D photonic integrated circuits (PICs), in addition to that of 2D PICs, which is similar to the pattern we have seen in the development of electronic integrated circuits. For creating 3D PICs, there are primarily two techniques. The first technique allows for freeform shaping of waveguides in any shapes and configurations thanks to ultrafast laser inscription (ULI). The second technique, multilayer stacking and coupling of planar PICs, makes use of relatively advanced 2D PIC fabrication procedures that are successively applied to each layer. There are benefits and drawbacks to both ways of fabricating 3D PICs, thus some applications might favour one over the other. The combination of 2D and 3D PICs, however, enables the creation of integrated microsystems with novel capabilities like non-mechanical beam steering, space-division multiplexing (SDM), programmable arbitrary beam shaping, and photonic signal processing. Examples of 3D PICs and 2D/3D integrated PICs are discussed in relation to two applications: Optical beam steering with optical phased arrays and SDM employing orbital-angular-momentum (OAM) multiplexing/demultiplexing. A 2D PIC has difficulties in supporting both polarizations even though it can act as an OAM multiplexer or demultiplexer on its own. A 3D PIC made by ULI, on the other hand, can effortlessly accommodate both polarizations with little propagation loss.

Keyword: Ultrafast laser inscription • Three-dimensional photonics • Photonic integrated circuits

Introduction

Our ability to process information has continued its astonishing trend of exponential expansion. Microsystem integration that is scalable, high-yield, and reasonably priced is necessary to sustainably support such fast expansion. More than 50 years ago, Moore's law predicted that the number of transistors that could be cheaply added to an electronic integrated circuit (EIC) would double roughly every two years for two-dimensional electronic integrated circuits (2D EICs). Dennard's law stated as a corollary that power efficiency will scale at the same rate as Moore's law. Although the extraordinary exponential scalability in integration has lasted for fifty years, Dennard's law, which had for forty years kept up with Moore's law, began to falter in 2004. Because there is no known technology solution below the 7-nm technology, where complementary metal-oxide semiconductor (CMOS) scaling is predicted to end, the International Technology Roadmap for Semiconductors (ITRS) refers to a "red brick wall" (as already noted, CMOS power density scaling stopped in 2004). Due to the fact that atoms do not scale with CMOS, there are two primary reasons for these limits: the increased leakage currents at such small scales, and the limitations of electronics in interconnects (because of the skin effects and impedances of electronic interconnects).

Literature Review

The chip multicore computers in 2006 gave these restrictions a brief relief by enabling parallel processing in multicores without increasing the clock speed. CMOS for silicon, hetero junction bipolar transistor (HBT) and high-electron mobility transistor (HEMT) for III-V platforms, and other electronic integration counterparts have always been used by photonic integration platforms because the electronics industry market is more than four times larger than the photonics counterpart. So it was no accident that the idea of co-integrating photonics and electronics appeared in the form of CMOS-photonics for silicon and optoelectronic integrated circuits (OEICs) for III-V. More significantly, heterogeneous integration has recently been sought after by both PICs and EICs. Modern EICs frequently combine heterogeneous circuits that use analogue and digital technology or circuits with silicon CMOS and Ge bipolar transistors [1]. Likewise, combining heterogeneous materials is advantageous for photonic integration. Silicon lacks the optical gain, Pockels effect, and Faraday Effect, which are necessary for creating lasers, phase modulators, and non-reciprocal devices, despite silicon photonics' quick rise to prominence as a practical and potentially ubiquitous photonic integration platform. Therefore, the functions of heterogeneously integrated microsystems can be significantly improved by co-integrating silicon with III-V materials, electro-optical dielectrics, and magneto-optical materials. The silicon substrate proves to be the most cost-effective and scalable as a substrate for an integration platform. The 450-mm silicon wafer platform for the CMOS EIC industry is being developed using the 14 nm gate CMOS technology, and 7 nm CMOS technology has just been shown. Silicon photonics is also making significant progress as a platform for the integration of photonic devices. It is well known that the availability of high-quality and dense passivation available from silicon's natural oxide, SiO_2, is the primary factor behind the successful and practical development of multibillion-transistor circuits based on silicon CMOS [2]. It's interesting to note that silicon photonics also benefits from the high-quality silicon dioxide used to create low-loss, high-contrast Si/SiO_2 waveguides by taking advantage of the low-loss interface between silicon and SiO_2. The majority of the integration work in PICs and EICs has been done in 2D to date. High-density integration has expanded to 3D integration by stacking many layers of 2D EICs utilising through-silicon vias because there are more than 10 billion transistors on per die (TSVs). In comparison to 2D EICs, three-dimensional EICs offered a variety of performance improvements, mostly due to less electrical wire being needed. They often provide (a) less power consumption since fewer repeaters and equalisers are required over shorter

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Received: 01 August, 2022; Manuscript No. jees-22-83985; **Editor Assigned:** 03 August, 2022, PreQC No. P-83985; **Reviewed:** 17 August, 2022, QC No. Q-83985; **Revised**: 23 August, 2022, Manuscript No. R-83985; **Published:** 31 August, 2022, DOI: 10.37421/2332-0796.2022.11.39

communication lengths, (b) less noise and jitter on shorter interconnects, and (c) higher packing density in 3D. We have also coined the phrase "photonic Moore's Law" to describe the rapid advancements in 2D photonic integrated circuits (PICs) in photonics. Recent advances in 3D photonic integration have become crucial milestones toward giving microsystems new capabilities and greater levels of integration. For example, 3D photonic integration-based space division multiplexing (SDM) overcomes 2D photonics' constraints in handling the spatial degree of freedom and polarisation dependence brought on by the requirement that all waveguides lie inside the same 2D plane. Diverse and complementary functionalities will be provided in a compact footprint via heterogeneous 2D and 3D photonic integration. This study summarises and projects the future of heterogeneous 2D and 3D photonic integration technologies [3].

Heterogeneous integration in two dimensions: Monolithic *vs.* hybrid

Either monolithic integration or hybrid integration can be used to achieve heterogeneous integration. Because it can make use of huge host substrates (like silicon wafers) and epitaxially produce III-V or other compound materials at a wafer scale at dimensions determined by the host substrate, monolithic integration by hetero-epitaxy is particularly appealing. For instance, even when high-quality InP wafers are restricted to 75 mm diameters, InP lasers can be achieved across 450-mm silicon wafers. However, overcoming the lattice mismatch and achieving hetero-epitaxially grown low-defect materials have been the key obstacles. Such flaws have been confined within small apertures using epitaxial lateral overgrowth (ELO) technology, which has also produced reasonably high-quality crystals on top of dielectrics that were laterally seeded from the host materials through the apertures. In addition, more recent research has shown record performance on all silicon-based lasers by utilising the 3D confinement of quantum dots to stop carriers from moving to dislocations. Another recent study using the rapid-melt-growth (RMG) technique showed that high-quality germanium crystal growth can be achieved from the deposition of an amorphous germanium layer followed by rapid thermal annealing (melting), which is seeded by subsurface silicon atoms reachable through nano-apertures created similarly to those used for ELO [4]. However, because to twin formations in III-V materials, the RMG approach is less effective for III-V compound semiconductors on silicon. Overall, obtaining low-defect heterogeneous integration through monolithic integration by heteroepitaxy is still difficult. Contrary to monolithic integration, hybrid integration technologies make use of various bonding processes between dissimilar (or comparable) materials that have already been formed on separate substrates instead of attempting material growth. Microelectronics is familiar with three types of interlayer bonding: (1) bonding without one, which includes (1a) anodic, (1b) direct, and (1c) low-temperature van der Waals bonding; (2) bonding with a metallic interlayer, which includes (2a) eutectic, (2b) thermos-compressive, and (2c) solder bonding; and (3) bonding with an insulating interlayer, which includes (3a) glass frit and (3 The most widely used bonding techniques for optoelectronics have been adhesive bonding (3b) and direct bonding (1b) (hydrophobic or hydrophilic). The variety of materials available for wafer-scale integration is often constrained by the difference in thermal expansion coefficients and wafer diameters, and both direct bonding and adhesive bonding provide adaptable heterogeneous integration across disparate materials. Depending on how the surfaces were treated before the bonding, direct bonding might be hydrophilic or hydrophobic. The hydroxyl of the atom produces water vapour after forming a hydrophilic connection. Assuming silicon wafer to silicon wafer bonding, the following are the early steps in this process:

$$Si - OH + Si - OH = Si - O - Si + H_2O$$

The silicon subsequently reacts with the water vapour to produce hydrogen gas: $Si + 2H_2O = SiO_2 + 2H_2$. Without oxides, hydrogenated or fluorinated surfaces will bond in a hydrophobic bond and release hydrogen gas: $Si - H + Si - H = Si - Si + H_2$. As a result, defects can be created in both situations when hydrogen gas is trapped at the interfaces, but this can be prevented by adding vertical out-gas channels with silicon oxide to absorb the hydrogen molecules [5]. In comparison to hydrophilic bonding, which has a bonding temperature of 350°C and an oxide layer at the bonding interface, hydrophobic bonding necessitates higher bonding temperatures (>550 °C), but it also produces stronger surface bonding energy (>2 J m^2) and close electrical connection. Due to the comparatively flexible requirements for the flatness of the bonding surfaces, adhesive bonding employing BenzoCycloButene (BCB), U-8 or other interface layers has become quite popular. InP/InGaAsP edge-emitting lasers have been created via hydrophobic direct bonding on GaAs substrates, AlGaAs/GaAs edge-emitting lasers have been created using Si substrates, and vertical cavity lasers with InP/InGaAsP active areas have been created using GaAs/AlAs distributed Bragg reflectors. AlInGaAs/InP-on – SOI hybrid lasers, modulators, and detectors have been created using hydrophilic direct bonding, and they achieve high-quality results without any obvious evidence of further defect-induced degradations. However, the current flows are restricted to the III-V regions and cannot cross the bonding interface.

Three-dimensional technologies

Multiple layers of 2D EICs are stacked and combined to form 3D EICs utilising TSVs. Similar to this, one kind of 3D PICs has made use of the orderly stacking of multilayer 2D photonic crystals [6]. A different kind of 3D PIC made use of the repetition of the combined processes of waveguide core layer deposition, lithography, etching, waveguide cladding layer deposition, and planarization (for instance, chemical and mechanical polishing) to finish multilayer 3D PICs where interlayer coupling could be made possible by low-loss inverse taper waveguides. These 3D PICs can also be created by wafer bonding two 2D PICs made of the same material or different material and using vertical couplers with interlayer optical coupling using inverse taper waveguides. A recent work has made it possible to fabricate photonic, electronic, and fluidic through-silicon vias in the same chip, demonstrating how the interlayer optical coupling can also take advantage of photonic vias that are similar to electrical TSVs.

The creation of 3D waveguides using ultrafast laser inscription may result in the most remarkable 3D PICs without an electronic counterpart (ULI). Waveguides can be directly written with a laser using a dielectric material, which is a very potent production method. It makes use of the multi-photon nonlinear absorption of sub-band gap photons to alter the structure of a substance in a way that is as long-lasting as the wavelength of the writing laser (for instance, about 1 ~ m^3). Refractive index and a higher susceptibility to chemical etching are two examples of the structural alterations. A nonlinear absorption mechanism drives the high-intensity region at the focus of a lens, where the generated alterations from a femtosecond train of optical pulses are highly confined in three dimensions. ULI has been widely shown in a variety of materials, such as amorphous glasses and crystals, with observed propagation losses of 0.3 dB cm^{-1} in fused silica, comparable to the 0.1 dB cm^{-1} propagation loss in 2D PICs (for example, Ge-doped silica on silicon) [7]. Additionally, recent experiments revealed that laser writing speeds on the order of 30 mm s^{-1} make it simple to produce high-quality three-dimensional waveguides. Finally, by modifying the geometry and make-up of the engraved waveguide. using multiple scan techniques or the beam shaping of the engraver laser, optical mode sizes can be tailored for a specific purpose [8].

Discussion and Conclusion

The rate of heterogeneous integration will quicken as a result of the continued trend of exponential development in data communications and processing. Along with the development of 2D PICs, we anticipate a significant increase in the rate of 3D PIC development. Due to its potential to create waveguides with arbitrarily curved contours and forms, the first technique using ULI is anticipated to have considerable demand among the two primary ways for producing 3D PICs. We anticipate increased efforts to create speedier inscription recipes or to split laser beams for parallel and simultaneous writing of numerous PICs due to the serial and sequential nature of its writing process. The availability of planar waveguide fabrication foundries will help to some extent to support the demand for the second 3D PIC production method using multilayer planar waveguides. We anticipate that the promising results in SDM coherent optical communications and optical beam steering achieved by

heterogeneously integrated 2D and 3D PICs will lead to novel applications in emerging fields such as spatial imaging, parallel optical connections, and light detection and ranging (LIDAR).

Acknowledgement

None.

Conflict of Interest

None.

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How to cite this article: Hao, Guangbo. "Photonic Integrated Heterogeneous 2 Dimensional/3 Dimensional Microsystems." J Electr Electron Syst 11 (2022): 39.