**Short Communication**
Volume 9:3, 2020

**Telecommunications System & Management**

**Open Access**

# High precision automatic mask-wafer aligner using moire sensing technology

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## Abstract

With the tremendous increase in complexity of integrated circuits having many multifunctional devices on the same board, rapidly shrink the interconnection line width to sub micro meter dimensions levels. The reduced device size can result in the reduced intrinsic switching time, the reduced power consumption as well as the reduced device cost. The devices dramatic miniaturization depends on novel lithographic processes and a high accuracy in mask-wafer alignment technique. Moire signal sensing technology can provide ultrahigh alignment accuracy up to less than +/- 50 nm. To achieve high accuracy in mask-wafer alignment, it required initial alignment to be done with the help of microscopes to bring the mask-wafer alignment grating pitch marks within the moire signal capture range. We have proposed two steps with coarse and fine mask-wafer alignment to make the process automatic without a microscope. When a laser beam is passed through a pair of identical gratings, of say 25 nm pitch, a relative displacement in their position gives a highly periodic signal called “moire” signal. This moire signal is suitably amplified, processed and digitalized to find out the maximum and the minimum values of the moire signal to compute its inverted moire signal Iinv and their difference error signal Idiff using Iinv = A + B – I and Idiff = Iinv – I = (A + B) – 2I, where A, B, and I are maximum, minimum and instantaneous digital values of the moire signal. A novel method was developed to align mask and wafer with placement accuracy estimated to be +/- 40 nm to achieve automatic alignment accuracy to be better than +/- 50 nm. Figure 1 and figure 2 show a setup for feasibility experiments with moire signals and digitalized moire signals with alignment marks, respectively.

### Biography

Brahm Pal Singh completed his Ph.D. in Quantum Electronics in 1990 from IIT Delhi, and D.Eng. in Quantum Engineering in 1996 from Nagoya University with Postdoctoral Stud- ies at NPL New Delhi, India and AIST Tsukuba, Japan. Dr. Singh is a Research & Development Manager in Advanced Technologies Development Center, ES Company, Panasonic Corporation. He has published over 30 research papers in reputed journals and international conferences/ symposiums and has been serving as a referee for the international reputed journals.

Note: This work is partly presented at joint event on annual epigenetics conference & international conference on mechatronics, automation and systems engineering (November 28-29, 2018 | Tokyo, Japan)