

## For How Long Should Effective Burn-in Testing Last?

Suhir E<sup>1,2,3\*</sup>

<sup>1</sup>ERS Co., 727 Alvina Ct., Los Altos, CA 94024, USA

<sup>2</sup>Portland State University, Portland, OR 97403, USA

<sup>3</sup>Technical University, Vienna, A-1040, Austria

Boltzmann-Arrhenius-Zhurkov (BAZ) model, suggested about fifty years ago in the kinetic theory of the strength of solids as a generalization of the Arrhenius' theory of chemical reactions and Boltzmann's statistical mechanics theory, is employed in this analysis for the assessment of the time required to conduct successful burn-in testing (BIT) of an electronic product. Although our analysis does not suggest any straight forward way of how to optimize BIT, it nonetheless sheds useful light on the significance of some important factors that affect the BIT time and should be considered when quantifying the BIT outcome. These factors include the role and significance of the random statistical failure rate (SFR) of the mass-produced components that the product under test is comprised of; the way to assess, using failure-oriented-accelerated-test (FOAT) data, the activation energy of the "freak" population; the role of the applied "external" stressor(s), if any; but, most importantly- the probabilities of the "freak" failures and the corresponding duration of the BIT effort. The analysis is an extension of the author's recently published *Aerospace* "to burn-in or not to burn-in" article.

No matter how good the design methodology or the manufacturing technology might be, there is always a possibility that a portion of the manufactured devices is not robust enough. If shipped to the customer, such "freaks" will most likely fail in actual operation conditions. This makes BIT an important reliability technique aimed at eliminating "freaks" prior to shipping the manufactured products to the customer(s) [1-4]. BIT is supposed to weed out unreliable "freaks" by operating all the manufactured devices for a predetermined (more or less arbitrary, but based on the establish practice) time under predetermined (also, to a great extent, arbitrary) elevated loading (usually, elevated temperature). BIT is expensive and labor-and-time consuming. In addition, there is always jeopardy that a long and extensive BIT might not only eliminate "freaks", but could inflict permanent damage to the "healthy" population of the manufactured devices. BIT is therefore a highly undesirable undertaking in electronic manufacturing. The recently published paper [5] can be of help when deciding on whether BIT effort is necessary or does not have to be conducted at all. If such testing is determined to be appropriate (although, as has been mentioned, there are no more or less trustworthy and established guidelines for doing that), its level and duration need to be decided upon beforehand. While the analysis below does not provide concrete guidelines for doing that, it nonetheless sheds useful light on the significance of some important factors that affect BIT. These factors include the role and significance of the random statistical failure rate (SFR) of the mass-produced components that the product under test is comprised of; the way to assess, using failure-oriented-accelerated-test (FOAT) data, the activation energy of the "freak" population; the role of the applied "external" stressor(s), if any; but, most importantly- the probabilities of the "freak" failures and the corresponding duration of the BIT effort. In summary, this analysis is an attempt to quantify, on the probabilistic basis, the outcome of a BIT-related FOAT [6-8].

Highly focused and highly cost effective FOAT is a special type of accelerated testing. It is aimed at confirming the anticipated physics of failure and at the assessment of the probability of failure and the corresponding time-to-failure (TTF). Clearly, the expected TTF is shorter, if the specified probability of failure is lower. FOAT should be conducted regardless of whether such a failure is extremely undesirable, which is the case in actual operation conditions, or, on the contrary, is highly desirable, when BIT is aimed at getting rid of the infant mortality portion (IMP) of the bathtub curve (BTC) is conducted.

FOAT should be geared to a flexible and physically meaningful constitutive equation, and BAZ equation [9-14]

$$\tau = \tau_0 \exp\left(\frac{U_0 - \gamma\sigma}{kT}\right) \quad (1)$$

can be employed in this capacity. Here  $\tau_0$  is the time constant,  $U_0, eV$ , is the basic (stress-free) activation energy, which is the material or device characteristic,  $T, ^\circ K$ , is the absolute temperature,  $k = 8.61733 \times 10^{-5} eV / ^\circ K$  is Boltzmann's constant, and  $\gamma$  is the sensitivity factor for the external loading.

The original BAZ model (1) [11,12] addressed a fracture mechanics problem and considered, in addition to the effect of the elevated temperature, also the external mechanical stress (per unit volume)  $\sigma$  as the only external stressor, not accounted for in the Arrhenius and Boltzmann's models. The stress  $\sigma$  in the original BAZ model is always mechanical, always tensile and the considered experimental specimens are always notched ones made of different materials. The BAZ model was recently generalized and extended [15] for the case of multiple stressors (stimuli), typical for microelectronics applications, such as thermal, stresses, elevated voltage or current, elevated humidity, random vibrations, light output, etc., and its effective use was demonstrated in a number of recent publications (see, e.g., [14]), when there was a need (an intent) to predict, on the probabilistic basis, the "remaining useful lifetime" (RUL) of an electronic or a photonic product, using the probabilistic design for reliability (PDR) concept [14-17]. Another important modification introduced to the original BAZ model (1) is the replacement of the time constant  $\tau_0$  with an expression that considers the role of time and the parameter that characterizes, in a particular

\*Corresponding author: Suhir E, Department of Mechanics and Materials, Electrical and Computer Engineering, Portland State University, Portland, OR 97207, USA, Tel: +650-969-1530; E-mail: [suhire@aol.com](mailto:suhire@aol.com)

Received May 06, 2019; Accepted May 23, 2019; Published May 31, 2019

Citation: Suhir E (2019) For How Long Should Effective Burn-in Testing Last? J Electr Electron Syst 8: 305. doi: [10.4172/2332-0796.1000305](https://doi.org/10.4172/2332-0796.1000305)

Copyright: © 2019 Suhir E. This is an open-access article distributed under the terms of the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original author and source are credited.

problem, the degree of degradation leading to failure. In the situation in question it is the variance  $D$  of the random statistical failure rate of the mass-produced components that the product of interest is comprised of.

It has been recently shown [5] that the answer to the fundamental “to burn-in or not to burn-in” question in electronics manufacturing could be based on the magnitude of the time derivative of the initial failure rate (at the beginning of the IMP of the BTC) of a newly fabricated product. It has been shown also that this derivative is, in effect, the variance (taking with a “minus” sign) of the random SFR of the electronic components that the manufactured products are comprised of. It was assumed that this random SFR was normally distributed between zero and infinity. This is a natural assumption, since the normal distribution is characterized, as is known, by the largest entropy. In the opposite extreme case, when the variance of the random SFR is significant (also with the “minus” sign, of course), this means that the “freaks” are very weak, and the BIT process, although needed, could be very short and of a low magnitude. This happens, when the area between the IMP of the BTC and the time axis is very narrow, i.e., when this portion “clings” (adheres as if glued firmly) to the vertical axis. Accordingly, the probability of the device non-failure, when BIT is conducted, could be sought in the form:

$$P = \exp \left[ -\gamma_t D I_* t \exp \left( -\frac{U_0 - \gamma_\sigma \sigma}{kT} \right) \right] \quad (2)$$

Here  $D$  is the variance of the random SFR of the mass-produced components that the manufactured product of interest is comprised of,  $I_*$  is the measured/monitored signal (such as, e.g., leakage current, whose agreed upon high value  $I_*$  is viewed as an indication of failure),  $t$  is time,  $\sigma$  is the “external” stressor,  $U_0$  is the highest activation energy (unlike in the original BAZ model, this energy may or may not be affected by the level of the external stressor),  $T$  is temperature,  $\gamma_\sigma$  is the stress sensitivity factor and  $\gamma_t$  is the time sensitivity factor. In the simplest case the stressor  $\sigma$  can be put equal to zero, i.e., the original Boltzmann-Arrhenius formula could be used. In such a case it has to be assumed that elevated temperatures always speed up the degradation process. It is well known, however, that the elevated thermal stresses arise in electronic devices and assemblies, comprised of dissimilar materials with different coefficients of thermal expansion (CTE), at low, not at elevated, temperatures, because it is at low (room, testing, operation) temperatures, when the deviation from the manufacturing temperature, at which these stresses are considered zero, is the largest. In the kinetic BAZ theory it is suggested that the temperature level affects the long-term aging of the material, while it is the external stress, which could be thermal stress that affects its short-term reliability. So, the stress  $\sigma$  in (2) could be thermal stress, but could be also, as has been indicated above, any other stressor (stimulus), like, e.g., elevated voltage, or current, or radiation, or humidity.

The equation (2) makes physical sense. Indeed, the probability of non-failure decreases with an increase in the variance  $D$ , the time  $t$ , the level  $I_*$  of the leakage current at failure and the environmental temperature  $T$ , and increases with an increase in the activation energy  $U_0$  value that characterizes the propensity of the material or the device to failure.

From (2) we obtain:  $\frac{dP}{dt} = -\frac{H(P)}{t}$ , where  $H(P) = -P \ln P$  is the entropy of the distribution. These formulas explain the reliability physics underlying the double-exponential distribution (2): the probability of non-failure of the BIT is proportional to the entropy of this distribution and is inversely proportional to the time of testing or operation. The

entropy  $H(P) = -P \ln P$  is zero for  $P = 0$  and for  $P = 1$ , and reaches its maximum value  $H_{\max} = e^{-1}$  for  $P = e^{-1}$ . Comparing this result with (2), one concludes that the maxima of the probability of non-failure and the entropy of the distribution (2) take place at the moment of time

$$t = \frac{1}{\gamma_t D I_*} \exp \left( \frac{U_0 - \gamma_\sigma \sigma}{kT} \right) \quad (3)$$

that can be considered as the mean time to failure (MTTF). This time is shorter for larger variance  $D$  of the SFR of the mass-produced components that the product under BIT is comprised of, for higher specified leakage current  $I_*$  at failure, for higher environmental temperature  $T$ , and for the lower effective activation energy  $U = U_0 - \gamma_\sigma \sigma$ . These trends make physical sense.

There are three unknowns in the expressions (2) and (3): the product  $\rho = \gamma_t D$  of the variance  $D$  and the time-sensitivity factor  $\gamma_t$ , the stress-sensitivity factor  $\gamma_\sigma$  and the activation energy  $U_0$ . Here how these unknowns could be determined from a two-step highly focused and highly cost-effective FOAT.

At the first step testing should be carried out for the same level of external loading (i.e., for the same level of the effective activation energy  $U = U_0 - \gamma_\sigma \sigma$ ), but for two different temperatures,  $T_1$  and  $T_2$ . Then the following relationships will be obtained:

$$P_{1,2} = \exp \left[ -\rho I_* t_{1,2} \exp \left( -\frac{U_0 - \gamma_\sigma \sigma}{kT_{1,2}} \right) \right] \quad (4)$$

Here  $P_{1,2}$  are the measured probabilities of non-failure,  $t_{1,2}$  are the corresponding times and  $I_*$  is the leakage current that is considered as an indication of the occurred failure. Since the numerator  $U = U_0 - \gamma_\sigma \sigma$  in the relationships (4) is kept the same, the amount  $\rho$  can be found as

$$\rho = \exp \left[ \frac{1}{\theta - 1} \left( \frac{n_2^\theta}{n_1} \right) \right], \quad (5)$$

Where

$$n_{1,2} = -\frac{\ln P_{1,2}}{I_* t_{1,2}} \theta = \frac{T_2}{T_1} \quad (6)$$

After the product  $\rho = \gamma_t D$  is determined, the second step of testing should be conducted at two different external stress levels  $\sigma_1$  and  $\sigma_2$  to determine the sensitivity factor  $\gamma_\sigma$ . If the stresses  $\sigma_1$  and  $\sigma_2$  are thermal stresses predicted for the testing temperatures  $T_1$  and  $T_2$ , they could be determined using a suitable analytical thermal stress model. Numerous predictive models have been developed and confirmed by FEA for various electronic assemblies and packages [18-21]. Then the stress sensitivity factor can be evaluated as:

$$\gamma_\sigma = k \frac{T_1 \ln n_1 - T_2 \ln n_2 + (T_2 - T_1) \ln \rho}{\sigma_1 - \sigma_2} \quad (7)$$

If, however, the external stress is not a thermal stress, then the temperatures at these tests should preferably be kept the same. Then the  $\rho$  value will not affect the factor  $\gamma_\sigma$ , and this factor could be evaluated by a simple formula

$$\gamma_\sigma = \frac{kT}{\sigma_1 - \sigma_2} \ln \left( \frac{n_1}{n_2} \right), \quad (8)$$

Where  $T$  is the testing temperature.

Finally, after the product  $\rho$  and the sensitivity factor  $\gamma_\sigma$  are determined, the activation energy can be found as

$$U_0 = -kT_1 \ln\left(\frac{n_1}{\rho}\right) + \gamma\sigma_1 = -kT_2 \ln\left(\frac{n_2}{\rho}\right) + \gamma\sigma_2 \quad (9)$$

The time to failure (TTF) can be determined from (2) as

$$t = \frac{-\ln P}{\rho I_*} \exp\left(\frac{U_0 - \gamma_\sigma \sigma}{kT}\right) \quad (10)$$

and the MTTF as

$$t = \frac{1}{\rho I_*} \exp\left(\frac{U_0 - \gamma_\sigma \sigma}{kT}\right) \quad (11)$$

These formulas indicate particularly that the probability-of-non-failure dependent TTF and the probability of non-failure independent MTTF are related as

$$\frac{TTF}{MTTF} = -\ln P. \quad (12)$$

As has been shown above, these two times coincide for  $P = e^{-1} = 0.3679$ . The ratio (12) changes from zero to infinity, when the probability  $P$  of non-failure changes from one to zero.

Let, e.g., the following FOAT data were obtained at the first step of FOAT:

1) After  $t_1 = 14h$  of testing at the temperature of  $T_1 = 60^\circ C = 333^\circ K$ , 90% of the tested devices reached the critical level of the leakage current of  $I_* = 3.5\mu A$  and, hence, failed, so that the recorded probability of non-failure is  $P_1 = 0.1$ ; the applied stress is elevated voltage  $\sigma_1 = 380V$ .

2) After  $t_2 = 28h$  of testing at the temperature of  $T_2 = 85^\circ C = 358^\circ K$ , 95% of the tested samples failed, so that the recorded probability of non-failure is  $P_2 = 0.05$ . The applied stress is still an elevated voltage of  $\sigma_1 = 380V$ .

Then the formulas (6) yield:

$$n_1 = -\frac{\ln P_1}{I_* t_1} = -\frac{\ln 0.1}{3.5 \times 14} = 4.6991 \times 10^{-2} \mu A^{-1} h^{-1};$$

$$n_2 = -\frac{\ln P_2}{I_* t_2} = -\frac{\ln 0.05}{3.5 \times 28} = 3.0569 \times 10^{-2} \mu A^{-1} h^{-1};$$

$$\theta = \frac{T_2}{T_1} = \frac{358}{333} = 1.0751$$

and the formula (5) results in the following value of the parameter  $\rho$ :

$$\begin{aligned} \rho &= \exp\left[\frac{1}{\theta - 1} \left(\frac{n_2^\theta}{n_1}\right)\right] = \\ &= \exp\left[\frac{1}{0.0751} \left(\frac{0.030569^{1.0751}}{0.046991}\right)\right] = \\ &= 785.3197 \mu A^{-1} h^{-1} \end{aligned}$$

At the second step of FOAT one can use, without conducting additional testing, the following information from the first step:

1) After  $t_1 = 14h$  of testing at the temperature of

$T = 60^\circ C = 333^\circ K$ , 90% of the tested devices reached the critical level of the leakage current of  $I_* = 3.5\mu A$  and, hence, failed, so that the recorded probability of non-failure is  $P_1 = 0.1$ ; the applied stress is still an elevated voltage of  $\sigma_1 = 380V$ .

2) After  $t_2 = 36h$  of testing at the same temperature of  $T = 60^\circ C = 333^\circ K$ , 98% of the tested samples failed, so that the probability of non-failure is  $P_2 = 0.02$ . The applied stress is an elevated voltage of  $\sigma_2 = 220V$ .

Then the first formula in (6) yields:

$$n_2 = -\frac{\ln P_2}{I_* t_2} = -\frac{\ln 0.02}{3.5 \times 36} = 3.1048 \times 10^{-2} \mu A^{-1} h^{-1};$$
 and the equation (8)

results in the following stress sensitivity factor:

$$\begin{aligned} \gamma &= kT \frac{\ln\left(\frac{n_1}{n_2}\right)}{\sigma_1 - \sigma_2} = \\ &= 8.61733 \times 10^{-5} \times 333 \frac{\ln\left(\frac{4.6991 \times 10^{-2}}{3.1048 \times 10^{-2}}\right)}{380 - 220} = \\ &= 7.4326 \times 10^{-5} eVxV^{-1} \end{aligned}$$

After the sensitivity factors are found, the activation energy can be determined as

$$\begin{aligned} U_0 &= -kT \ln\left(\frac{n_1}{\rho}\right) + \gamma\sigma_1 = -8.61733 \times 10^{-5} \times 333 \times \\ &\times \ln\left(\frac{4.6991 \times 10^{-2}}{785.3197}\right) + 7.4326 \times 10^{-5} \times 380 = \\ &= 0.2790 + 0.0282 = 0.3072 eV \end{aligned}$$

or as

$$\begin{aligned} U_0 &= -kT \ln\left(\frac{n_2}{\rho}\right) + \gamma\sigma_2 = -8.61733 \times 10^{-5} \times 333 \times \\ &\times \ln\left(\frac{3.1048 \times 10^{-2}}{785.3197}\right) + 7.4326 \times 10^{-5} \times 220 = \\ &= 0.2909 + 0.0164 = 0.3072 eV \end{aligned}$$

No wonder that these values are considerably lower than the activation energies of healthy electronic products. Many manufacturers feel ("rule of thumb") that the level of 0.7eV can be used as an appropriate tentative number for the activation energy of healthy electronic devices. The calculated data show also that the stress-free activation energy slightly increases with an increase in the level of loading. This increase is about 5-8% in the carried out examples.

The formula (11) results in the following MTTF value:

$$\begin{aligned} t &= \frac{1}{\rho I_*} \exp\left(\frac{U_0 - \gamma_\sigma \sigma}{kT}\right) = \\ &= \frac{1}{785.3197 \times 3.5} \exp\left(\frac{0.3072 - 7.4326 \times 10^{-5}}{8.61733 \times 10^{-5} \times 333}\right) = \\ &= 16.1835 h \end{aligned}$$

The TTF is the probability of non-failure dependent and can be found as

$$t = \frac{-\ln P}{\rho I_*} \exp\left(\frac{U_0 - \gamma_\sigma \sigma}{kT}\right) = MTTF_x(-\ln P)$$

The calculated BIT TTF for different probabilities of non-failures are shown in Table 1:

P	0.005	0.0075	0.01	0.05
TTF, h	85.7453	79.1835	74.5278	48.4814

Table 1: TTF vs Probability-of-Non-Failure.

## Conclusion

Although our analysis does not suggest any straightforward way of how to optimize BIT, it nonetheless sheds useful light on the significance of some important factors that affect the BIT time and should be considered when quantifying the BIT outcome. These factors include the role and significance of the random statistical failure rate (SFR) of the mass-produced components that the product under test is comprised of; the way to assess, using failure-oriented-accelerated-test (FOAT) data, the activation energy of the “freak” population; the role of the applied “external” stressor(s), if any; but, most importantly- the probabilities of the “freak” failures and the corresponding duration of the BIT effort.

## References

1. Kececioglu D, Sun FB (1997) Burn-in-Testing, Prentice Hall.
2. Jordan J, Pecht M, Fink J (1997) How Burn-in Can Reduce Quality and Reliability. Int J of Microcircuits and Electronic Packaging 20: 35-40.
3. Crowe D, Feinberg A (2001) Design for Reliability (Electronics Handbook Series), 1st ed., CRC Press.
4. Vichare N, Pecht M (2006) Prognostics and Health Management of Electronics, IEEE CPMT Transactions.
5. Suhir E (2019) To Burn-In, or Not to Burn-in: That’s the Question. Aerospace.
6. Suhir E (2011) Remaining Useful Lifetime (RUL): Probabilistic Predictive Model Int PHM J 2: 1-5.
7. Suhir, E (2013) Failure-Oriented-Accelerated-Testing (FOAT) and Its Role in Making an aerospace electronics device into a product. J Mater Sci-Mater El.
8. Suhir E (2014) HALT, FOAT and Their Role in Making a Viable Device into a Reliable Product. IEEE-AIAA Aerospace Conf.
9. Suhir E (2013) Could Electronics Reliability Be Predicted, Quantified and Assured? Microelectronics Reliability 53: 925-936.
10. Suhir E, Mahajan R, Lucero A, Bechou L (2012) Probabilistic Design-for-Reliability Concept and Novel Approach to Qualification Testing of Aerospace Electronic Products, Proc. IEEE Aerospace Conference.
11. Zhurkov SN (1957) The Problem of the Strength of Solids, Vestn. Akad. Nauk SSSR (*Bulletin of the USSR Academy of Sciences*) 11: 78-82.
12. Zhurkov SN (1965) Kinetic Concept of the Strength of Solids. Int. J. Fracture Mechanics 1 311–323.
13. Suhir E, Kang SM (2013) Boltzmann-Arrhenius-Zhurkov (BAZ) Model in Physics-of-Materials Problems. Modern Physics Letters B, vol: 27.
14. Suhir E (2019) Failure Oriented Accelerated Testing (FOAT), Boltzmann Arrhenius Zhurkov Equation (BAZ), and their Application in Aerospace Microelectronics and Photonics Reliability Engineering. Int J Aeronautics Aerospace Res 6: 185-191.
15. Suhir E, Bensoussan A (2014) Aerospace optoelectronics reliability: Application of multi-parametric BAZ model. Proc IEEE Aerospace Conference.
16. Suhir E (2010) Probabilistic Design for Reliability. Chip Scale Reviews.
17. Suhir E, Mahajan R (2011) Are Current Qualification Practices Adequate? Circuit Assembly.
18. Suhir E (2019) Analytical Thermal Stress Modeling in Electronics and Photonics Engineering: Application of the Concept of Interfacial Compliance. Journal of Thermal Stresses.
19. Suhir E (2018) Analytical Thermal Stress Model for a Typical Flip-Chip Package Design. J Mater Sci-Mater El 29: 2676-2688.
20. Suhir E (2013) Thermal Stress Failures in Electronics and Photonics: Physics, Modeling. Prevention J Thermal Stresses, vol: 36.
21. Suhir E (2009) Analytical Thermal Stress Modeling in Electronic and Photonic photonics engineering: Application of the concept of interfacial compliance. J Thermal Stresses 62: 29-48.