Journal of
Electrical & Electronic Systems

Zhou and Yuan, J Electr Electron Syst 2013, 3:1
DOI: 10.4172/2332-0796.1000e112

Editorial Open Access

Design Techniques for High-Speed I/Os: Challenges and Opportunities

Yushi Zhou and Fei Yuan*

Department of Electrical and Computer Engineering, Ryerson University, Canada

Abstract

This editorial examines design techniques for high-speed serial data links over wire channels. The state-of-the-art of serial links over wire channels is briefly studied. The imperfections of wire channels at high frequencies and their effect on multi-Gbps serial links are examined. It is followed with a close examination of modulation schemes effective in combating the effect of the finite bandwidth of wire channels. Channel equalization, both pre-emphasis and post-equalization, are investigated with an emphasis on adaptive decision feedback equalization. Challenges and opportunities in combating ISI are explored.

Introduction

Although f_T of MOS transistors has well exceeded 100 GHz, the speed of data links are rather low, as shown in Table 1 [1-13], mainly due to Inter-Symbol Interference (ISI) caused by channel imperfections including finite channel bandwidth, reflections, and cross-talks. Although low-loss backplanes are desirable, they are prohibitively costly. Combating channel imperfections by means of electrical signaling, data modulation and encoding, and channel equalization has been proven to be effective, robust, and economical. This paper examines challenges encountered in and design techniques for multi-Gbps data communication over wire channels, and explores opportunities and solutions to improve the performance of data links. The remainder of the paper is organized as follows: Section 2 investigates the imperfections of wire channels and their impact on multi-Gbps data links. Section 3 studies modulation schemes effective in minimizing the effect of the limited bandwidth of wire channels and cross-talks among neighboring channels. Channel equalization that compensates for the effect of finite channel bandwidth, reflection, and crosstalk is addressed in Section 4. Concluding remarks are drawn in Section 5.

Channel Characteristics

The characteristics of wire channels are determined by the elements of the channels such as vias, traces and connectors, and environment in which the channels reside such as boards and neighboring devices [14-16]. The limited bandwidth of wire channels due to the resistive and dielectric loss of the channels at high frequencies gives rise to frequency-dependent attenuation of data symbols traveling along the channels.

References	Tech. [nm]	Channel loss [dB]	Data rate [Gb/s]
Dickson, et al. [1]	45	-21	10
Nazari, et al. [2]	45	-25	15
Gangasaniet, al. [3]	45	-32	16
Agrawal, et al. [4]	45	-25	19
Amirkhany, et al. [5]	40	-10	16
Kaviani, et al. [6]	40	-15	20
Quan, et al. [7]	40	-26	14
Joy et al. [8]	40	-34	16
Cui, et al. [9]	40	-20	23
Toifl, et al. [10]	32	-27	12.5
Toifl, et al. [11]	32	-36	30
Bulzacchelli, et al. [12]	32	-35	28
J. Savoj, et al. [13]	28	-33	12.5

Table 1: Data rates of serial links over wire channels. Channel Loss is measured at half baud-rate frequency.

Impedance discontinuities of channels, typically occurring at vias, connectors, and packages, cause reflection. Crosstalk at both the near and far-end of channels arising from capacitive and inductive coupling between the channels and neighboring devices also undermines signal integrity. All contributes to ISI that reduces the opening of data eyes and yields a poor Bit Error Rate (BER). The frequency response of a wire channel typically consists of a smooth roll-off section at low frequencies and deepening toughs from capacitive impedance discontinuities and crests from inductive impedance mismatches at high frequencies. As a result, at the receiver end, data symbols typically consist of pre-cursors, a main cursor, and post-cursors. For severely lossy channels, the number of post-cursors is significantly larger as compared with that of the pre-cursors. For reflective channels with strong impedance discontinuities located far away from the transmitters, large post-cursors exist both near and far away from the main cursor with a large number of insignificant small post-cursors in between. The characteristics and behavior of these channels differ fundamentally from those with only high dispersion thereby requiring different compensation schemes in channel equalization.

Modulation Schemes

Although a large number of modulation schemes exist for wireless communications, only a handful modulation schemes have been successfully deployed for multi-Gbps data communications over wire channels to combat channel imperfections. Perhaps the most widely used modulation scheme in backplane applications is Pulse Amplitude Modulation (PAM) with 2PAM the most power and silicon efficient. Although 2PAM enjoys the largest noise margins subsequently the best BER, it suffers from the drawback of poor spectral efficiency. As compared with 2PAM, 4PAM trades voltage spacing for spectral efficiency. Both transmitters and receivers of 4PAM data links are considerably more complex as compared with those of 2PAM data links, mainly due to the

***Corresponding author:** Fei Yuan, Department of Electrical and Computer Engineering, Ryerson University, 350 Victoria Street, Toronto, Ontario, Canada M5B 2K3, Tel: 416-979-5000; Fax: 416-979-5280; E-mail: fyuan@ryerson.ca

Received December 05, 2013; **Accepted** December 09, 2013; **Published** December 11, 2013

Citation: Zhou Y, Yuan F (2013) Design Techniques for High-Speed I/Os: Challenges and Opportunities. J Electr Electron Syst 3: e112. doi:10.4172/2332-0796.1000e112

need for a Digital-to-Analog Converter (DAC) at the transmitters, an Analog-to-Digital Converter (ADC) at the receiver, and complex clock recovery schemes [17-24]. High-order PAM was also used for wireline communications to improve spectral efficiency. For example, Foley and Flynn demonstrated a 1.3 Gb/s serial link in 0.5 m CMOS using 8PAM [25]. Song, et al. [26] proposed a 10 Gb/s transceiver with dual-mode 10PAM. The main difficulties encountered in deploying high-order PAM include reduced noise margins subsequently a poor BER, the need for high-speed power-greedy ADCs, and complex clock recovery circuitry.

Not only can data be modulated spatially to improve spectral efficiency, they can also be modulated temporally, i.e., data are represented by pulses with pulse width modulated by data (Pulse Width Modulation or PWM) [27-31]. As compared with PAM, PWM is less spectral efficient. For example, the worst symbol time of 4PWM is 4UI where UI is unit interval while the symbol time of 4PAM is constant and is one UI. When the both edges of PWM pulses are used to carry data information, the symbol time of 4PWM is reduced to 2 UIs [31]. Want, et al. proposed a dual-edge PWM to improve channel efficiency, especially highly lossy channels [31]. PWM was also used as pre-emphasis to boost the high frequency components of data symbols prior to their transmission [27,29]. PWM that utilizes the orthogonal characteristics of Walsh codes was also used in serial links to transmit multiple Walsh-code encoded data symbols via the same channel simultaneously [32]. Pulse-width-amplitude modulation (PWAM) that utilizes the advantages of both PAM and PWM simultaneously to further improve data rates by modulating data symbols both spatially and temporally becomes attractive [28,33-38]. For example, 4PAM and 4PWM transmit 2 bits per symbol while 4PWAM transmits 4 bitsper symbol. Note the symbol time of 4PWAM is the same as 2PWM.

Modulation schemes also found their applications in parallel data links. For example, in [39], the transmitter utilized Analog Multi-Tone (AMT) to achieve 24 Gbps in 90 nm CMOS. A three-level differential encoding was used to obtain higher I/O pin efficiency [40]. A Code-division-Multiple-Access (CDMA) based transceiver was proposed for parallel links to improve crosstalk rejection [41]. Kossel, et al. showed that the use of Tomlinson-Harashima pre-coding initially proposed in [42,43] at transmitters can remove post-cursor ISI [44].

The preceding investigation demonstrates that an effective means to combat ISI caused by channel imperfections is to utilize advanced modulation schemes to alleviate bandwidth constraint on channels. For example, the orthogonal characteristics of CDMA enable the transmission of multiple data via parallel links with the minimum crosstalk among them. The orthogonality identity of Walsh codes allows multiple Walsh-code encoded data symbols to be transmitted to the same channel simultaneously without interfering each other. More research is clearly needed in deploying advanced modulation and data-encoding schemes popular in wireless communications for Gbps data links.

Channel Equalization

Due to channel imperfections, data symbols received at the far end of the channel consist of pre-cursors, a main cursor, and post-cursors. The main cursor represents the transmitted data and is used for data recovery while precursors and post-cursors must be removed by means of channel equalization. Boosting the high-frequency components [45,46] or attenuating the low-frequency components of data symbols prior to their transmission, known as pre-emphasis, are effective [47,48]. Since the former deteriorates crosstalk, the latter is generally preferred. Near-end channel equalization is usually implemented using a finite impulse response filter that introduces zeros at the location of the dominant poles of the channels so as to cancel the poles [20,49]. The order of pre-emphasis filters is low, usually limited to 4, indicating that typical wire channels can be adequately modeled using a 4th-order low-pass when reflection and cross-talk are not accounted for [50,51]. Since the characteristics of the channel are not known prior to data transmission, the optimal tap coefficients of pre-emphasis filters cannot be obtained a prior, revealing the rigidness of pre-emphasis. Another intrinsic limitation of pre-emphasis is its inability to remove ISI caused by reflection and crosstalk, which are particularly important when data rate is high and channels contain multiple impedance discontinuities. Far-end channel equalization combats ISI by amplifying the high-frequency components of received data symbols or subtracting the estimated post-cursors from data symbols prior to clock and data recovery, often both simultaneously. Similar to pre-emphasis, Continuous-Time Linear Equalizers (CTLEs) provide zeros to cancel out the dominant poles of the channels so that the equalized channel exhibits the desired all-pass characteristic. CTLE is often deployed in conjunction with nonlinear post-equalization [51,52]. It is also used solely for channels with negligible reflection and crosstalk [53,54]. Because the received symbol is severely attenuated, input offset voltage compensation is typically required in CTLE [55,56]. Unlike CTLE, nonlinear post-equalization removes post-cursors by subtracting estimated post-cursors directly from data symbols prior to slicing. Perhaps the most widely used nonlinear equalization is Decision Feedback Equalization (DFE) [57]. As compared with CTLE, DFE does not deteriorate crosstalk. Also, since the taps of DFE can be adjusted in accordance with the opening of data eyes or the power of the error between the input and output of the slicer, it is most effective and robust in eliminating ISI caused by finite channel bandwidth, reflection, and crosstalk. As DFE has no effect on pre-cursors, it is usually deployed together with pre-emphasis to remove both pre-cursors and post-cursors.

DFE operations include data slicing, multiplication, and subtraction. All need to be completed within one UI for tap-1. Loop-unrolling has been proven to be an effective technique in meeting the timing constraint of the tap-1 of DFE [19,58-60]. High-order loop-unrolling also emerged when data rate exceeds 10 Gb/s, however, at the cost of high silicon consumption [10,11,61]. To relax the timing constraint and at the same time to lower the power consumption of the remaining DFE taps, the half rate approach is widely used [59]. Quarter-rate approach was also deployed to further relax the timing constraint, however, at the cost of high silicon consumption [10,11,49,61]. Since DFE operation is based on the correct recovery of data, an error occurring in data slicing will propagate through the delay chain of the equalizer and affect subsequent data recovery decisions. To mitigate this, the input of the slicer must be sufficiently large and disturbance-free. Current-integrating is proven to be effective in eliminating transient disturbances in data symbols prior to slicing [62,63]. Using CTLE prior to slicing to boost data symbols is also effective [7,52,64]. To minimize the kick-back of slicers, slicers should also be multistage configured [65,66]. To speed up multiplication and summation operations, current-steering multiplication is widely used for its speed. For the same reason, current mode summation including current-integrating summers that offer the key advantage of high-speed and low power consumption is widely preferred [52,67-69].

The variation of the characteristics of wire channels requires the tap coefficients of DFE be set adaptively in accordance with the characteristics of the channels. Least Mean Square (LMS) updates

tap coefficients in such a way that the power of the error between the output and input of the slicer is minimized [70]. Sign-Sign LMS (SS-LMS) where only the sign of the error and data symbol are used in search for optimal tap coefficients are widely used due to its ease of implementation and fast convergence. Alternatively, the opening of data eyes can be used to guide DFE search [71,72]. Eye-opening can be captured using an Eye-Opening Monitor (EOM) [73-81]. Jitter-based eye-opening monitors that minimize timing jitter at the edges of data eyes also emerged [82]. Dual-mode adaptive DFE consisting of a data-DFE to maximize vertical opening and a jitter-DFE to minimize timing jitter outperforms EOM-based DFE [49]. For highly reflective channels, large post-cursors might exist at taps both close to and far away from the main cursor with a large number of small post-cursors between them. Equalizing these channels using conventional DFE requires a large number of taps, resulting in high power and silicon consumption even though taps corresponding to the insignificant post-cursors contribute little to channel equaliation. Floating-tap DFE proposed in [7,64,83] is an elegant technique in eliminating reflection-induced post-cursors located far away from the main cursor.

The preceding study shows that the adaptivity of DFE should address the following key issues in DFE-based channel equalization: (i) Optimal tap coefficients to provide the complete cancellation of post-cursors. (ii) Optimal number of taps to minimize power and silicon consumption. (iii) Optimal distribution of taps to remove noncritical taps so as to minimize the number of taps and achieve the best channel equalization without sacrificing power and silicon resources. Although SS-LMS is widely used in search for these optimal parameters, EOM and jitter-based DFE demonstrates promising performance and power efficiency especially they unify DFE and CDR into one operation.

Conclusions

The imperfections of wire channels and their impact on multi-Gbps data links were examined. It was followed by a close examination of modulation schemes effective in combating the effect of channel imperfections. Channel equalization, both pre-emphasis and post-equalization, were investigated with an emphasis on adaptive decision feedback equalization. Challenges and opportunities in combating ISI were explored. We showed that two directions of research that could result in improved performance of data links are advanced modulation and data-encoding schemes and adaptive channel equalization.

Acknowledgement

Financial support from the Natural Science and Engineering Research Council of Canada is gratefully acknowledged by the authors.

References

1. Dickson T, Liu Y, Rylov S, Dang B, Tsang C, et al. (2012) An 8x 10-Gb/s source-synchronous I/O system based on high-density silicon carrier interconnects. IEEE J Solid-St Circ 47: 884-896.
2. Nazari M, Emami-Neyestanak A (2012) A 15-Gb/s 0.5-mW/Gbps two-tap DFE receiver with far-end crosstalk cancellation. IEEE J Solid-St Circ 47: 2420-2432.
3. Gangasani G, Hsu C, Bulzacchelli J, Rylov S, Beukema T, et al. (2012) A 16-Gb/s backplane transceiver with 12-tap current integrating DFE and dynamic adaption of voltage offset and timing drifts in 45-nm SOI CMOS technology. IEEE J Solid-St Circ 47: 1828-1841.
4. Agrawal A, Dickson JBT, Liu Y, Tierno J, Friedman D (2012) A 19-Gb/s serial link receiver with both 4-tap FFE and 5-tap DFE function in 45-nm SOI CMOS. IEEE J Solid-St Circ 47: 2.
5. Amirkhany A, Kaviani K, Abbasfar A, Fazeel S, Beyene W, et al. (2012) A 4.1-pJ/b, 16-Gb/s coded differential bidirectional parallel electrical link. IEEE J Solid-St Circ 47: 3208-3219.
6. Kaviani K, Wu T, Wei J, Amirkhany A, Shen J, et al. (2012) A tri-modal 20-Gbps/link differential/DDR3/GDDR5 memory interface. IEEE J Solid-St Circ 47: 926-937.
7. Zhong F, Quan S, Liu W, Aziz P, Jing T, et al. (2011) A 1.0625-to-14.025 Gb/s multimedia transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS. IEEE International Solid-State Circuits Conference Digests of Technical Papers, San Francisco, CA, USA, pp 348-349.
8. Joy A, Mair H, Lee H, Feldman A, Portmann C, et al. (2011) Analog-DFE-based 16 Gb/s SerDes in 40 nm CMOS that operates across 34 dB loss channels at Nyquist with a baud rate CDR and 1.2 Vpp voltage-mode driver. IEEE International Solid-State Circuits Conference Digests of Technical Papers, San Francisco, CA, USA, pp 350-351.
9. Cui D, Raghavan B, Singh U, Vasani A, Huang Z, et al. (2012) A dual-channel 23-Gbps CMOS transmitter/receiver for 40-Gbps RZ-DQPSK and CS-RZ-DQPSK optical transmission. IEEE J Solid-St Circ 47: 3249-3260.
10. Toifl T, Menolfi C, Ruegg M, Reutemann R, Dreps D, et al. (2012) A 2.6 mw/Gb/s 12.5 Gbps RX with 8-tap switched-capacitor DFE in 32 nm CMOS. IEEE J Solid-St Circ 47: 897-910.
11. A 3.1 mW/Gb/s 30 Gbps quadrater-rate triple-speculation 15-tap SC-DFE RX data path in 32 nm CMOS. Symposium on Circuits Digests of Technical Papers, Honolulu, HI, USA, pp 102-103.
12. Bulzacchelli J, Menolfi C, Beukema T, Storaska D, Hertle J, et al. (2012) A 28-Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32-nm SOI CMOS technology. IEEE J Solid-St Circ 47: 3232-3248.
13. Savoj J, Hsieh K, Upadhyaya P, An F, Bekele A, et al. (2012) A wide common-mode fully adaptive multi-standard 12.5 Gb/s backplane transceiver in 28 nm CMOS. Symposium on VLSI Circuits Digests of Technical Papers, Honolulu, HI, USA, pp 104-105.
14. Balan V, Caroselli J, Chern J, Chow C, Dadi R, et al. (2005) A 4.8-6.4-Gb/s serial link for backplane applications using decision feedback equalization. IEEE J Solid-St Circ 40: 1957-1967.
15. Savoj J, Hsieh K, Upadhyaya P, An F, Im J, (2012) Design of high-speed wireline transceivers for backplane communications in 28nm CMOS. Proc IEEE Custom Integrated Circuits Conference, pp 1-4.
16. Shahramian S, Yasotharan H, Carusone A (2012) Decision feedback equalizer architectures with multiple continuous-time infinite impulse response filters. IEEE T Circuits-II 59: 226-230.
17. Zerbe J, Werner C, Stojanovic V, Chen F, Wei J, et al. (2004) Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplane transceiver cell. IEEE J Solid-St Circ 38: 2121-2130.
18. Stojanovic V, Ho A, Garlepp B, Chen F, Wei J, et al. (2005) Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery. IEEE J Solid-St Circ 40: 1012-1026.
19. Bulzacchelli J, Meghelli M, Rylov S, Rhee W, Rylyakov A, et al. (2006) A 10-Gb/s 5-tap DFE/4-tap FFE transceiver in 90 nm CMOS technology. IEEE J Solid-St Circ 41: 2885-2900.
20. Yuan F (2009) An area-power efficient 4-PAM full-clock 10 Gb/s CMOS pre-emphasis serial link transmitter. Analog Integr Circ S 59: 257-264.
21. Lee J, Chen M, Wang H (2008) Design and comparison of three 20-Gb/s backplane transceivers for duobinary, PAM4 and NRZ data. IEEE J Solid-St Circ 43: 2120-2133.
22. Min B, Palermo S (2011) A 20Gb/s Triple-Mode (PAM-2,PAM-4, and duobinary) transmitter. Proceedings of IEEE Mid-West Symposium on Circuits and Systems, pp 1-4.
23. Stonick J, Wei G, Sonntag J, Weinlader D (2003) An adaptive PAM-4 5-Gb/s backplane transceiver in 0.25 µm CMOS. IEEE J Solid-St Circ 38: 436-443.
24. Toifl T, Menolfi C, Ruegg M, Reutemann R, Buchmann P, et al. (2006) A 22-Gb/s PAM-4 receiver in 90-nm CMOS SOI technology. IEEE J Solid-St Circ 41: 954-965.
25. Foley D, Flynn M (2002) A low-power 8-PAM serial transceiver in 0.5 µm digital CMOS. IEEE J Solid-St Circ 37: 310-316.
26. Song B, Kim K, Lee J, Burm J (2013) A 0.18-/spl µm CMOS 10-Gb/s dual-mode 10-PAM serial link transceiver. IEEE T Circuits I 60: 457-468.

27. Schrader J, Klumperink E, Visschers J, Nauta B (2006) Pulsewidth modulation pre-emphasis applied in a wireline transmitter, achieving 33 dB loss compensation at 5-Gb/s in 0.13-/spl µm CMOS. IEEE J Solid-St Circ 41: 990-999.

28. Yang C, Lee Y (2008) A PWM and PAM signaling hybrid technology for serial-link transceivers. IEEE T Instrum Meas 57: 1058-1070.

29. Cheng H, Musa F, Carusone A (2009) A 32/16-Gb/s dual-mode pulsewidth modulation pre-emphasis (PWM-PE) transmitter with 30-dB loss compensation using a high-speed CML design methodology. IEEE T Circuits I 56: 1794-1806.

30. Rashdan M, Yousif A, Haslett J, Maundy B (2010) Data link design using a time-based approach. Proceedings of the IEEE International Symposium on Circuits and Systems, pp 3977-3980.

31. Wang W, Buckwalter J (2013) A 10-Gb/s, 107-nW dual-edge pulse width modulation transceiver. IEEE T Circuits I (In press).

32. Al-Taee A, Yuan F, Ye A (2012) A new power-efficient CDMA based transmitter for high-speed serial links. Analog Integr Circ S 71: 343-348.

33. Yang C, Lee Y (2005) A 0.18-µm CMOS 1-Gb/s serial link transceiver by using PWM and PAM techniques. Proceedings of the IEEE International Symposium on Circuits and Systems, pp 1150-1153.

34. Tang R, Kim Y (2006) PWAM signaling scheme for high speed serial link transceiver design. Proceedings of the 16th ACM Great Lakes symposium on VLSI, New York, USA, pp 49-53.

35. Ghaderi N, Hadidi K (2009) A CMOS 32 Gb/s serial link transceiver using PWM and PAM scheme. Proceedings of the European Circuit Theory and Design, Antalya, Turkey, pp 205-208.

36. Kim Y, Kim Y (2010) Design and noise analysis of 8 Gb/s capacitive low power and high speed 4-PWAM transceiver. Proceedings of the IEEE Mid-West Symposium on Circuits and Systems, Seattle, WA, USA, pp 785-788.

37. Rashdan M, Haslett J (2013) Comparing performance of a multiple valued time-based serial data link with other serial links. Proceedings of the IEEE International Symposium on Multiple-Valued Logic, Toyama, Japan, pp 248-253.

38. Rashdan M, Yousif A, Haslett J (2013) Differential time signaling data-link architecture. J Sign Process Syst 70: 21-37.

39. Amirkhany A, Abbasfar A, Savoj J, Jeeradit M, Garlepp B, et al. (2008) A 24 Gb/s software programmable analog multi-tone transmitter. IEEE J Solid-St Circ 43: 999-1009.

40. Zogopoulos S, Namgoong W (2009) High-speed single-ended parallel link based on three-level differential encoding. IEEE J Solid-St Circ 44: 549-557.

41. Hsueh T, Su P, Pamarti S (2010) A 3x3.8Gb/s four-wire high speed I/Q link based on CDMA-like crosstalk cancellation. IEEE J Solid-St Circ 45: 1522-1532.

42. Tomlinson M (1971) New automatic equalizer employing modulo arithmetic. IEE Electronics Letters 7: 138-139.

43. Harashima H, Miyakawa H (1972) Matched-transmission technique for channels with intersymbol interference. IEEE T Commun 20: 774-780.

44. Kossel M, Toifl T, Francese P, Brandli M, Menolfi C, et al. (2013) A 10Gb/s 8-tap 6b 2-pam/4-pam Tomlinson-Harashima precoding transmitter for future memory-link applications in 22-nm SOI CMOS. IEEE J Solid-St Circ 48: 3268-3284.

45. Zhao Z, Wang J, Li S, Chen J (2007) A 2.5-Gb/s 0.13 µm CMOS current mode logic transceiver with pre-emphasis and equalization. Proceedings of the International Conference ASIC, pp 368-371.

46. Kao S, Liu S (2010) A 20-Gb/s transmitter with adaptive preemphasis in 65 nm CMOS technology. IEEE T Circuits II 57: 319-323.

47. Fiedler A, Mactaggart R, Welch J, Krishnan S (1997) A 1.0625 Gbps transceiver with 2x-oversampling and transmit signal preemphasis. IEEE International Solid-State Circuits Conference Digests of Technical Papers pp 238-239.

48. Dally WJ, Poulton J (1997) Transmitter equalization for 4-Gbps signaling. IEEE Micro 17: 48-56.

49. Wong K, Chen E, Yang C (2008) Edge and data adaptive equalization of serial-link transceivers. IEEE J Solid-St Circ 43: 2157-2169.

50. Lee M, Dally W, Farjad-Rad R, Ng H, Senthinathan R, et al. (2003) CMOS high-speed I/Os - present and future. Proceedings of the International Conference on Computer Design pp 454-461.

51. Balan V, Caroselli J, Chern J, Desai C, Liu C (2004) A 4.8-6.4 Gbps serial link for back-plane applications using decision feedback equalization. Proceedings of the IEEE Custom Integrated Circuits Conference pp 331-334.

52. Ying Y, Liu S (2011) A 20Gb/s digitally adaptive equalizer/DFE with blind sampling. IEEE International Solid-State Circuits Conference Digests of Technical Papers pp 444-446.

53. Gondi S, Razavi B (2007) Equalization and clock and data recovery techniques for 10 Gb/s CMOS serial-link receivers. IEEE J Solid-St Circ 42: 1999-2011.

54. Lee D, Han J, Han G, Park S (2009) 10 Gbit/s 0.0065 mm2 6 mW analogue adaptive equalizer utilizing negative capacitance. IET Electronics Letters 45: 863-865.

55. Hidaka Y, Gai W, Horie T, Jiang J, Koyanagi Y, et al. (2009) A 4-channel 1.25-10.3 Gb/s backplane transceiver macro with 35 dB equalizer and sign-based zero-forcing adaptive control. IEEE J Solid-St Circ 44: 3547-3559.

56. Kim B, Liu Y, Dickson T, Bulzacchelli J, Friedman D (2009) A 10-Gb/s compact low-power serial I/O with DFE-IIR equalization in 65-nm CMOS. IEEE J Solid-St Circ 44: 3526-3538.

57. Austin M (1967) Decision-feedback equalization for digital communication over dispersive channels. IEEE International Research Laboratory of Electronics Technical Report 461.

58. Krishna K, Yokoyama-Martin D, Caffee A, Jones C, Loikkanen M, et al. (2005) A multi-giga-bit backplane transceiver core in 0.13 µm CMOS with a power-efficient equalization architecture. IEEE J Solid-St Circ 40: 2658-2666.

59. Beukema T, Sorna M, Selander K, Zier S, Ji B, et al. (2005) A 6.4-Gb/s CMOS SerDes core with feed-forward and decision-feedback equalization. IEEE J Solid-St Circ 40: 2633-2645.

60. Leibowitz B, Kizer J, Lee H, Chen F, Ho A, et al. (2007) A 7.5Gb/s 10-tap DFE receiver with first tap partial response, spectrally gated adaptation, and 2nd-order data filtered CDR. IEEE International Solid-State Circuits Conference Digests of Technical Papers pp 228-599.

61. Toifl T, Ruegg TMM, Inti R, Menolfi C, Brandli M, et al. (2012) A 3.1 mW/Gbps 30 Gbps quarter-rate triple-speculation 15-tap SC-DFE RX data path in 32 nm CMOS. Symposium on VLSI Circuits Digests of Technical Papers pp 102-103.

62. Sidiropoulos S, Horowitz M (1997) A 700 Mb/s/pin CMOS signaling interface using current integrating receivers. IEEE J Solid-St Circ 32: 681-690.

63. Wang T, Yuan F (2007) A new current-mode incremental signaling scheme with applications to Gb/s parallel links. IEEE T Circuits I 54: 255-267.

64. Zhong F, Quan S, Liu W, Aziz P, Tai J, et al. (2011) A 1.0625-14.025 Gb/s multi-media transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS. IEEE J Solid-St Circ 46: 126-3139.

65. Carusone T, Johns D, Martin K (2012) Analog integrated circuit design (2nd edn.). Wiley and Sons, New York, USA.

66. Fayed A, Ismail M (2008) A low-voltage, low-power CMOS analog adaptive equalizer for UTP-5 cables. IEEE T Circuits I 55: 480-495.

67. Dickson T, Bulzacchelli J, Friedman D (2008) A 12 Gb/s 11 mW half-rate sampled 5-tap decision feedback equalizer with current integrating summers in 45 nm SOI CMOS technology. Symposium on VLSI Circuits Digests of Technical Papers pp 58-59.

68. Bulzacchelli J, Dickson T, Deniz Z, Ainspan H, Parker B, et al. (2009) A 78 mW 11.1Gb/s 5-tap DFE receiver with digitally calibrated current-integrating summers in 65nm CMOS. IEEE Internatinal Solid-State Circuits Conference Digests of Technical Papers pp 368-369.

69. Payandelhnia P, Abbasfar A, Sheikhaei S, Forouzandeh B, Nanbakhsh K, et al. (2011) A 4 mW 3-tap 10 Gb/s decision feedback equalizer. Proceedings of the IEEE Mid-West Symposium on Circuits and Systems pp 1-4.

70. Winters J, Gitlin R (1990) Electrical signal processing techniques in long-haul fiber-optic systems. IEEE T Comm 38: 1439-1453.

71. Payne R, Bhakta B, Ramaswamy S, Wu S, Powers J, et al. (2005) A 6.25Gb/s binary adaptive DFE with first post-cursor tap cancellation for serial backplane communications. IEEE Internatinal Solid-State Circuits Conference Digests of Technical Papers pp 68-69.

72. Payne R, Bhakta B, Ramaswamy S, Wu S, Powers J, et al. (2005) A 6.25-Gb/s binary transceiver in 0.13-µm CMOS for serial data transmission across high loss legacy backplane channels. IEEE J Solid-St Circ 40: 2646-2657.

73. Bien F, Kim H, Hur Y, Maeng M, Cha J, et al. (2006) A 10 Gb/s reconfigurable CMOS equalizer employing a transition detector-based output monitoring technique for band-limited serial links. IEEE T Microwave Theory Tech 54: 4538-4547.

74. Hyoungsoo K, de Ginestous J, Bien F, Lee K, Chandramouli S, et al. (2007) An electronic dispersion compensator (EDC) with an analog eye-opening monitor (EOM) for 1.25 Gb/s gigabit passive optical network (GPON) upstream links. IEEE T Microwave Theory Tech 55: 2942-2950.

75. Hong D, Cheng K (2007) An accurate jitter estimation technique for efficient high speed I/O testing. Proceedings of the Asian Test Symposium pp 224-229.

76. Chen L, Zhang X, Spagna F (2009) A scalable 3.6-5.2 mW 5-to-10 Gb/s 4-tab DFE in 32 nm. IEEE International Solid-State Circuits Conference Digests of Technical Papers, pp 180-181.

77. Spagna F, Chen L, Deshpande M, Fan Y, Gambetta D, et al. (2010) A 78 mw 11.8Gb/s serial link transceiver with adaptive RX equalization and baud-rate CDR in 32 nm CMOS. IEEE International Solid-State Circuits Conference Digests of Technical Papers, pp 366-367.

78. Pozzoni M, Erba S, Viola P, Pisati M, Depaoli E, et al. (2009) A multi-standard 1.5 to 10 Gb/s latch-based 3-tap DFE receiver with a SSC tolerant CDR for serial backplane communication. IEEE J Solid-St Circ 44: 1306-1315.

79. Suttorp T, Langmann U (2007) A 10-Gb/s CMOS serial-link receiver using eye-opening monitoring for adaptive equalization and for clock and data recovery. Proceedings of the IEEE Custom Integrated Circuits Conference, pp 277-280.

80. Sarvari S, Tahmoureszadeh T, Sheikholeslami A, Tamura H, Kibune M (2010) A 5 Gb/s speculative DFE for 2x blind ADC-based receivers in 65-nm CMOS. Symposium on VLSI Circuits Digests of Technical Papers pp 69-70.

81. Al-Taee A, Yuan F, Ye A, Sadr S (2013) New 2D eye-opening monitor for Gbps serial links. IEEE T VLSI Systems.

82. Gerfers F, Besten G, Petkov P, Conder J, Koellmann A (2008) A 0.2-2 Gb/s 6x OSR receiver using a digitally self-adaptive equalizer. IEEE J Solid-St Circ 43: 1436-1448.

83. Aziz P, Kimura H, Malipatil A, Kotagiri S (2012) A class of down sampled floating tap DFE architectures with application to serial links. Proc IEEE International Symposium on Circuits and Systems pp 325-328.