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Design and Simulation of Single-Phase Five-Level Symmetrical Cascaded H-Bridge Multilevel Inverter with Reduces Number of Switches

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Abstract

Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of ac waveforms. Such inverters synthesize a desired output voltage from several levels of dc voltages as inputs. This paper analyzes the performance of five level cascaded H-bridge multilevel inverter with reduce number of power switches. Further by reducing switches and increasing level will reduce filter cost & harmonic content. 5- Level cascaded H-bridge asymmetrical multilevel inverter topology requires 8 switches but in this new multilevel inverter it requires 6 switches in which same multilevel is obtained. Invariably switching losses and cost also reduced. In this paper only multilevel inverter circuitry will be studied. The performance has been analyzed by the MATLAB/Simulink.

Keywords: Cascaded multilevel inverter; SPWM; APOD; PD; POD; THD

Introduction

Basically, inverter is electrical devices that convert direct current (dc) input voltage to a symmetrical alternating current (ac) output voltage of desired magnitude and frequency. The output voltage could be fixed or variable at a fixed or variable frequency.

A variable output voltage can be obtained by varying the input dc voltage and maintain the gain of the inverter (ratio of the ac output voltage to the dc input voltage) constant.

Conversely, if the dc input voltage is fixed and is not controllable, a variable output voltage can be obtained by varying the gain of the inverter which is normally accompanied by pulse width modulator within the inverter [1]. The waveform of practical inverter are non-sinusoidal and contain some harmonic. Demerits of this inverter are less efficiency, high cost and high switching losses. To overcome these demerits lead to what is called multilevel inverters. This multilevel inverter does the same work as inverter, but on high power applications. This multilevel inverter is an electrical device that is capable of producing different voltage levels. The term multilevel inverter began with three levels converter. The multilevel converter has been introduced since 1975. The cascade H-bridge multilevel inverters was first suggested in 1975 (M. Kavita 2012) [2]. In past years multilevel inverters are used in high power and high voltage applications. Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform. The mL1 output voltage having less number of harmonics as compared to the conventional bipolar inverter output voltage. If the MLI output increase to N level, the harmonics reduced to the output voltage value to zero.

Multilevel inverters have several advantages as compared to conventional bipolar inverter in the following way.

1. Capability to operate at high voltage with lower dv/dt per switching.
2. High level efficiency.
3. Low electromagnetic interferences.
4. High magnitude sinusoidal voltage with extremely low distortion at fundamental frequency can be produced at the output with the help of MLI by connecting sufficient number of dc at input side.

The multilevel inverter includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms (F.Z. Peng 2003) [3,4]. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. However, if the number of levels is increases, the number of components required is more, this results into reduction of overall reliability and efficiency of power converter. On the other hand, solution with a low number of levels either need a rather large and expensive LC filter to limit the motor winding insulation stress or can only be used with motors that do withstand such stress. There are three main types of Multilevel Inverter. These are Diode clamped, Flying capacitor and Cascaded H-bridge Multilevel Inverter A m o n g these three, cascaded H-bridges multilevel has a modular structure and require least number of components as compared to diode-clamped and flying capacitor multilevel inverter, and as a result of this, it is widely used for many applications in electrical engineering [5].

From Figure 1 above, dc input voltage is the source of dc power devices, multilevel inverter (n-level) changes dc voltage to ac voltage and gating signal control system generates the pulse that control the switching pattern of the H-bridge MOSFET switches [6-9].

All researches work that has gone on inverter circuit configuration mainly in reducing the switches at higher voltage levels, by reducing switches and increasing voltage levels will reduce filter cost and harmonic content. Five-levels CHB MLI topology required Eight switches and two separate dc sources, but to reduce switching loss and cost, six switches required in which the same MLI output voltage is obtained. These CHB MLI with six switches and two batteries will improve output waveform and reduce total harmonic distortion. The circuit diagram of CHB MLI with six switches and two separate dc sources and its switching states

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is shown below Table 1. The core aim of this topology is to reduce number of switches. This 5-level inverter carries 6 switches in two legs, and three switches in each leg. The switches are named as S1, S2, S3, S4, S5 and S6. S1, S2, S3 are placed in first leg and S4, S5, S6 are placed in second leg as shown in Figure 2 below [10-13].

Switching Schemes with Operations

- For +2Vdc, switch S2, S4 and S6 are switched ON for getting maximum voltage (Figure 3)
- For +1Vdc, switch S2, S3 and S4 are switched ON for next priority level of voltage (Figure 4)
- For zero output voltage, switches S4, S5 and S6 are switched ON (Figure 5)
- For negative (-2Vdc) voltage switch S1, S3 and S5 are switched ON (Figure 6)
- For negative (-1Vdc) voltage, switch S1, S2 and S6 are switched ON (Figure 7)
- Pulses for 5-level symmetric CHB MLI (Figure 8)

Simulation Results

In this paper MATLAB, PROTEUS is used. Proteus is a real time software tool which is implemented before performing hardware. In MATLAB the five level inverter circuit is simulated and results of output voltage and THD is shown below Figure 9.

The GUI plots are used for the Fast Fourier Transforms (FFT) analysis to determine the Total Harmonic content (THD) Figures 10-12.

The simulation of 5-level is carried out in MATLAB SIMILINK. Total Harmonic distortion calculated, and is 23.20%. MOSFET are used in this design which has high voltage and current carrying capability. A gate driver circuit is to be used for boosting the pulses from a microcontroller PIC16F877A and is used for generating required pulses [13-17].

S/no	Switching sequences						Voltage levels
	S1	S2	S3	S4	S5	S6	
1	0	1	0	1	0	1	+2 Vdc
2	0	0	1	1	1	0	+1 Vdc
3	0	0	0	1	1	1	0 Vdc
4	1	1	0	0	0	1	-1 Vdc
5	1	0	1	0	1	0	-2 Vdc

Note: 1 indicates that switch is ON state,
0 indicates that switch is OFF state

Table 1: Switching states of modified 7-levels CHB MLI.

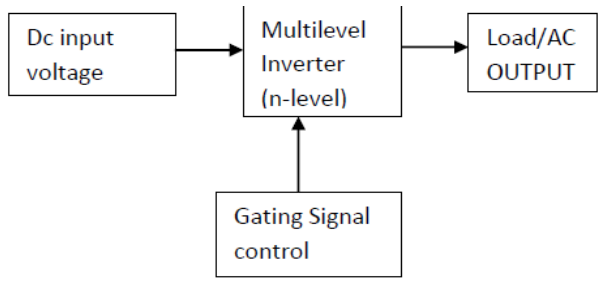

Figure 1: Multi-user Distributed Massive MIMO transceiver model system.

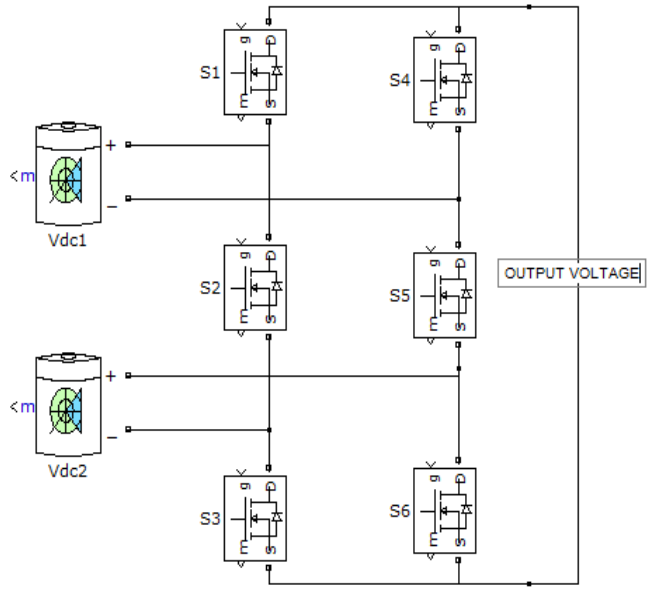

Figure 2: Circuit diagram of 5-level CHB MLI with reduced switches & dc sources.

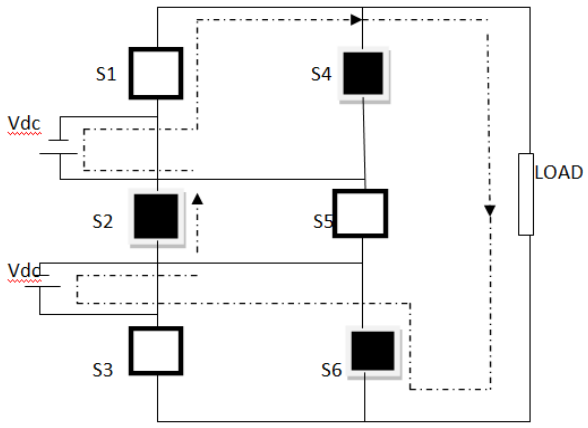

Figure 3: Switching sequences for getting a voltage +2Vdc.

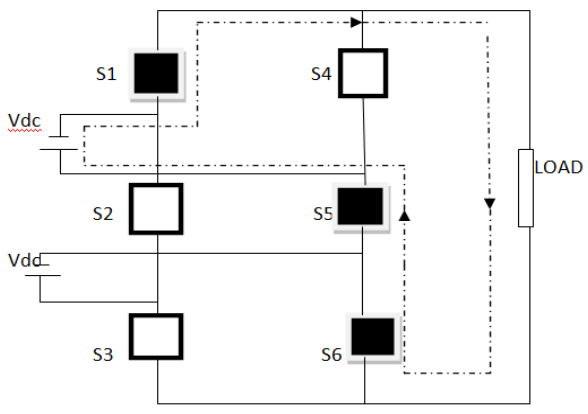

Figure 4: Switching sequence for getting a voltage +1Vdc.

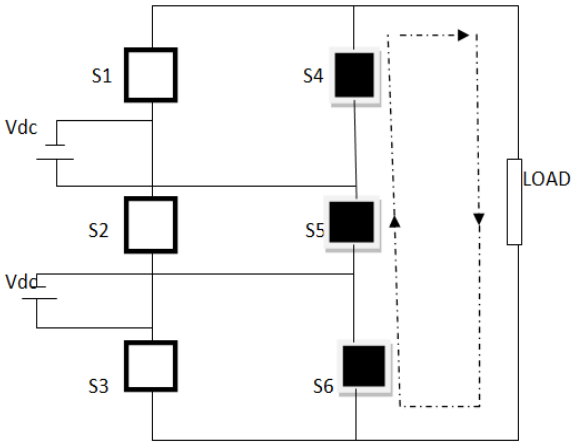

Figure 5: Switching sequence for getting a zero voltage.

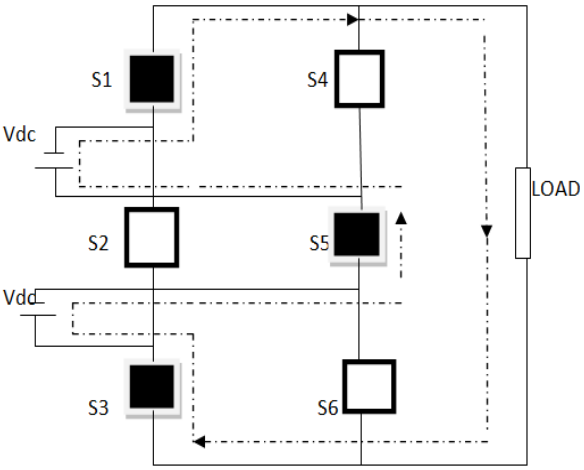

Figure 6: switching sequence for zero voltage.

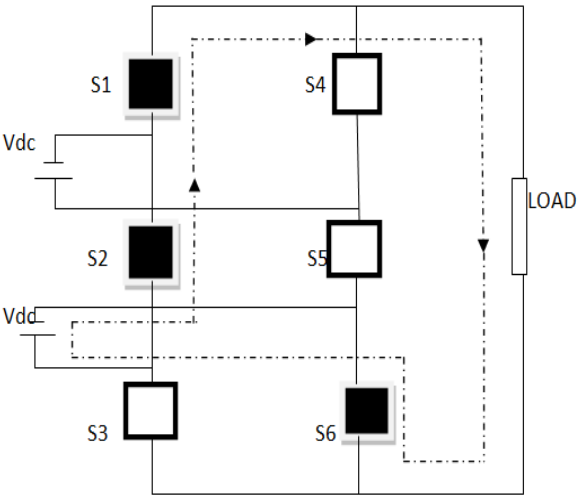

Figure 7: Switching sequence for getting -1Vdc voltage.

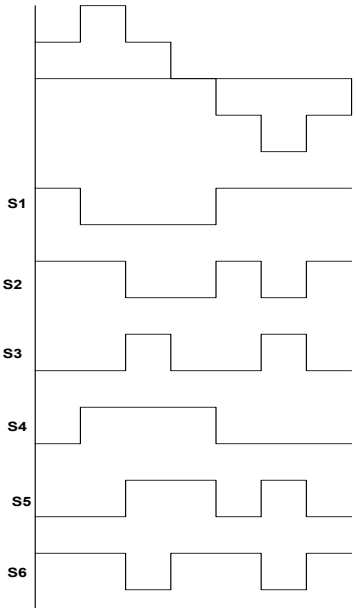

Figure 8: Triggering pulses for five level symmetric CHB MLI.

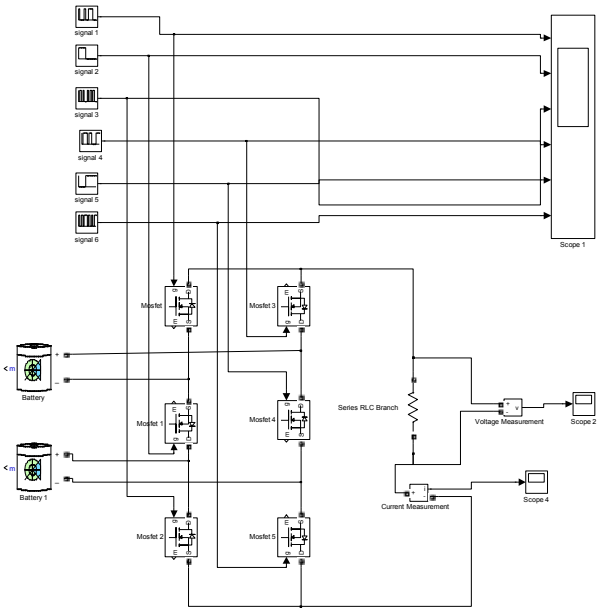

Figure 9: 5-level CHB MLI circuitry in MATLAB tool.

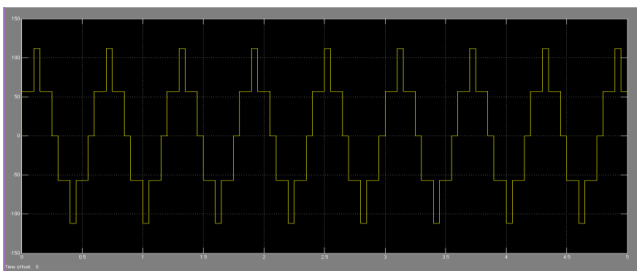

Figure 10: Output waveform of 5-levels single phase symmetric CHB MLI.

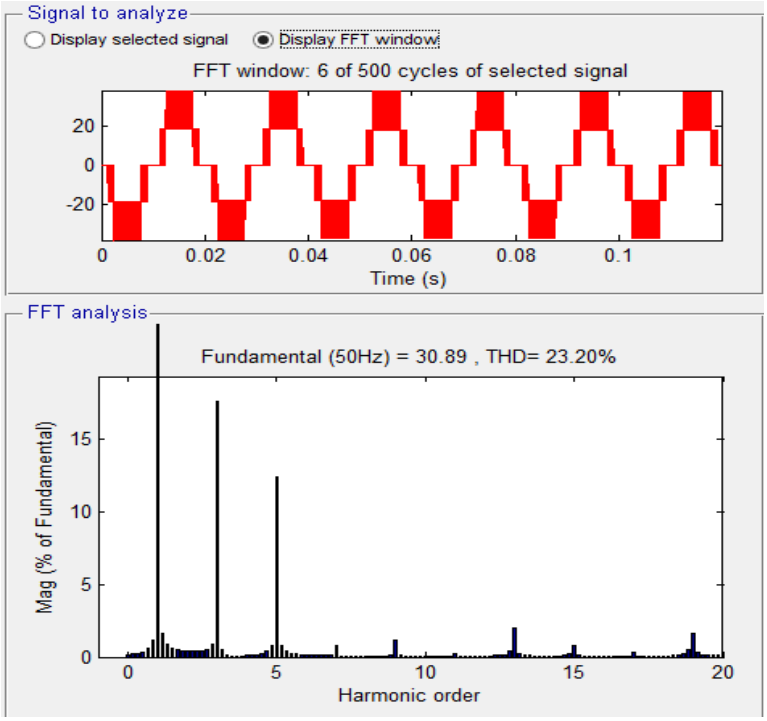

Figure 11: 5-levels THD in MATLAB tool.

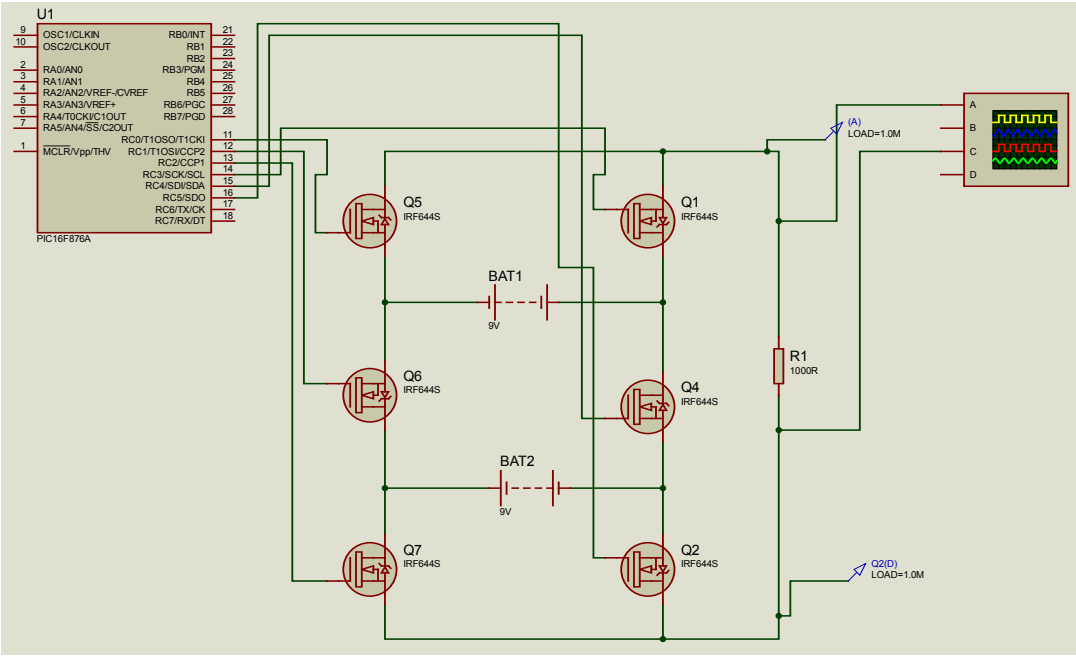

Figure 12: 5-level symmetric CHB MLI circuitry in proteous software.

Conclusion

This paper showed that this modified multilevel inverter topology with reduced number of switches can be implemented for industrial drive applications. This multilevel inverter structure and its basic operations have been analyzed. A detailed procedure for calculating required voltage level on each stage has been analyzed. As conventional five-level inverter involves eight switches, it increases switching losses; cost and circuit complexity. This 5-level inverter engages only six switches which reduces switching losses, cost and circuit complexity. Moreover it effectively reduces lower order harmonics. Therefore effective reduction of total harmonics distortion is achieved.

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