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Design and Implementation of Vedic Multipliers Using Reversible Logic Gates

Ravi JN*, Vijay Prakash AM and Madan S

Department of ECE, Bangalore Institute of Technology, Bangalore, India

Abstract

Implementing the already existing circuits or new circuits using reversible logic has drawn a significant interest in recent years as a promising computing technique having application in low power CMOS, quantum computing, nanotechnology, optical computing …etc. Reversible logic gates offer significant advantages such as high speed, low power, ease of fabrication …etc. Also, circuits designed using these circuits would have better performance as compared to existing circuits. Main goals of reversible logic synthesis are to minimize the garbage, to minimize the delay, to minimize the total number of gates, to minimize the width of the circuit. In this paper, designer implemented 2 × 2 and 4 × 4 bit Vedic multipliers using reversible logic gate.

Keywords: Vedic multiplier; Reversible logic gates; Circuits; Power consumption

Introduction

Basic concepts required to understand the reversible logic gates are described below:

Why reversible logic gates?

When a computational system erases a bit of information, it must dissipate (kTln2) Joules of energy, where, 'k' is the Boltzmann's constant and 'T' is the temperature which has been proved experimentally. For T=300k (room temperature), this is about 2.9×10^{-21} Joules [1]. This is roughly the kinetic energy of a single air molecule at room temperature. Today's computers will erase a bit of information, every time they perform a logic operation. These logic operations are therefore called "Irreversible". This erasure is done very efficiently and much more than (kT) Joules of energy is dissipated for each bit erased. If we are to continue the revolution in computer hardware performance, we must continue to reduce energy dissipated by each logic operation. It can be reduced, by improving conventional methods, i.e., by improving the efficiency by reducing the power dissipated [2].

An alternative approach is to use logic operations that do not erase information. These are called "Reversible logic" operations and in practical applications they can dissipate arbitrarily less heat. As the energy dissipated per irreversible logic operation approaches the fundamental limit of (kTln2) Joules, the use of reversible operations is likely to become more attractive. Hence, if we wanted to reduce energy dissipation per logic operation, below (kTln2) Joules, we will be forced to use reversible logic [3].

Basic reversible logic gates

There are different types of reversible logic circuits are available. In this paper, author has used two of them, namely-Feynman gate (FG) and peres gate (PG) [4]. Boolean expressions for each of those two gates are shown in block diagrams below, at each output pins (Figures 1 and 2).

Proposed Design Methodology

Different logic circuit can be realized by using reversible logic gates. This paper presents a better way to build a circuit which requires less power for its operation, lesser delay time…etc. Some of the design approaches for different logic circuits with reversible logic gates are below.

Design and implementation of 2 × 2 and 4 × 4 bit vedic multiplier using irreversible logic gates

Vedic multiplier technique is used to perform multiplication operation in a faster way as compared to usual multiplication approach. In this paper we tried to implement the same not using irreversible gates but with reversible gates [5-7]. Basically, 2 × 2 bit can be designed as shown in following figure, using irreversible logic gates. Then later peres gate is used as building block to gate to get Vedic multiplier (Figures 3 and 4).

Let A and B be 2 bit numbers which should be multiplied. Assuming each has bits as (a1a0) and (b1b0), we do following operation to get the product [8,9].

The final result will be c2s2s1s0. We can extend this procedure for higher bit multiplication using this 2 × 2 bit VM as building block. Similarly block diagram for 4 × 4 bit VM is shown below (Figure 5).

Figure 1: Basic block diagram of FG gate.

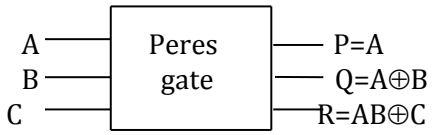

Figure 2: Basic block diagram of PG gate.

***Corresponding author:** Ravi JN, Department of ECE, Bangalore Institute of Technology, Bangalore, India, Tel: 08026615865; E-mail: ravijn095@gmail.com

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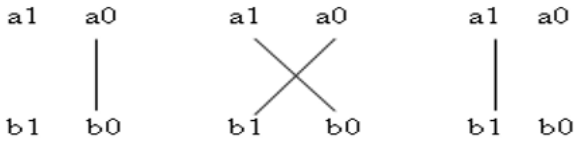

Figure 3: The vedic multiplication method for two 2-bit binary numbers.

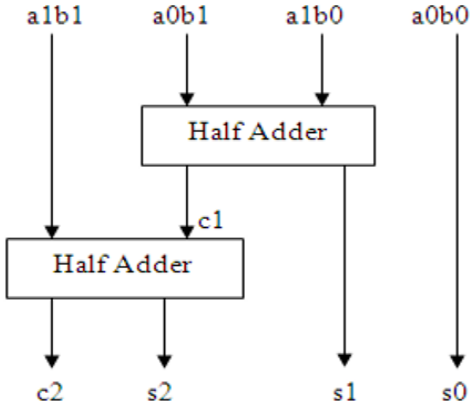

Figure 4: Block diagram of 2 × 2 bit vedic multiplier (VM).

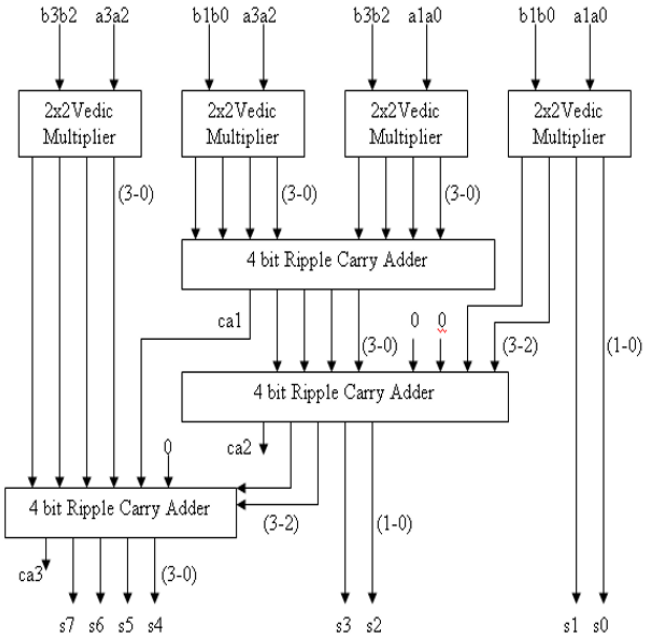

Figure 5: Block diagram of 4 × 4 bit vedic multiplier (VM).

Design and implementation of 2 × 2 and 4 × 4 bit vedic multiplier using reversible logic gates

Here we design VM using reversible logic gates, mainly we will use peres gate as building block to get VM.

As mentioned earlier circuits designed using reversible logic gates will consume less power [10]. Following figures shows the arrangement for 2 × 2 and 4 × 4 bit VM (in the case of 4 × 4 bit multiplier design we will use 2 × 2 bit VM. In general higher order bit VM can be implemented using 2 × 2 bit VM as building block) (Figure 6).

In the case of 4 × 4 bit VM we will use same block diagram as in Figure 2 with 4 bit ripple carry adder replaced with 4 bit adder using reversible gate (peres gate). Here 4 bit adder is implemented using peres gate which is used to realize full adder block as shown below (Figures 7 and 8).

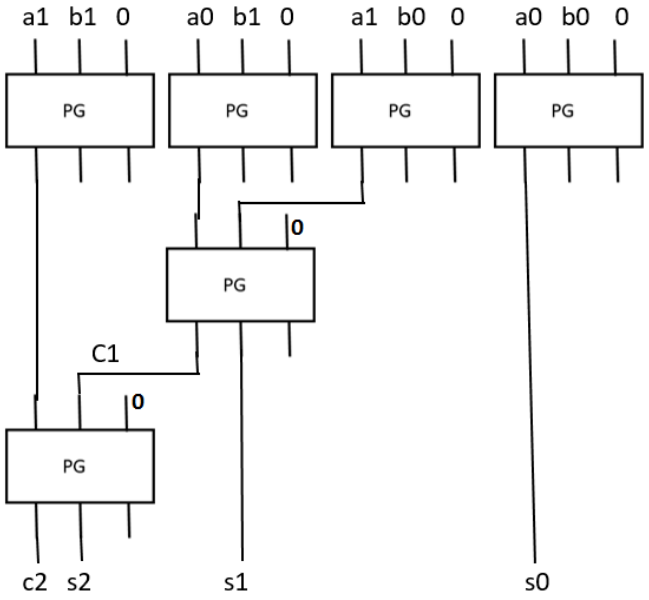

Figure 6: 2 × 2 bit VM using reversible logic gates.

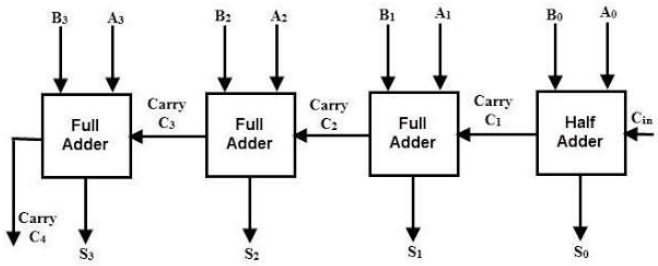

Figure 7: 4 Bit adder using 4 full adders.

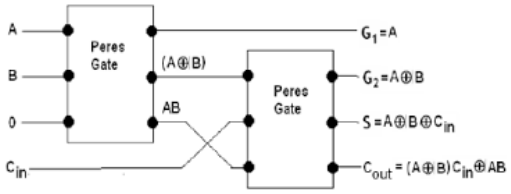

Figure 8: Full adder designed using peres gates.

Results and Conclusion

Simulation results

This section deals with the simulation results which are obtained for each circuit. The proposed circuits are simulated on Modalism tool and synthesized for Xilinx Spartan-3 with Device 3s4000fg208-5. For all the above mentioned circuits i.e., 2 × 2 and 4 × 4 bit VM functionality is verified by using Xilinx ISE 13.1 software. Results can be easily verified with the help of waveforms for each case. Simulated snapshot input, output waveforms of the proposed circuits are shown from Figures 9 and 10.

Synthesis results

Synthesis results for the above designed circuits are shown below in terms of delay generated out that circuit, power consumption. Results are simulated with the help of Xilinx software. Simulation results for 2 circuits discussed in this paper are shown below with the help of timing diagram using Xilinx software. Both circuits are tested for its functional correctness using Xilinx software. The simulation results are as shown in Tables 1-3.

Reversible circuits	Delay (ns)	Power (mw)
2 × 2 VM	7.858	60
4 × 4 VM	13.839	60

Table 1: Delay and power consumption of designed circuits.

Conclusion

In this paper, author discussed about 2 × 2 and 4 × 4 bit VM

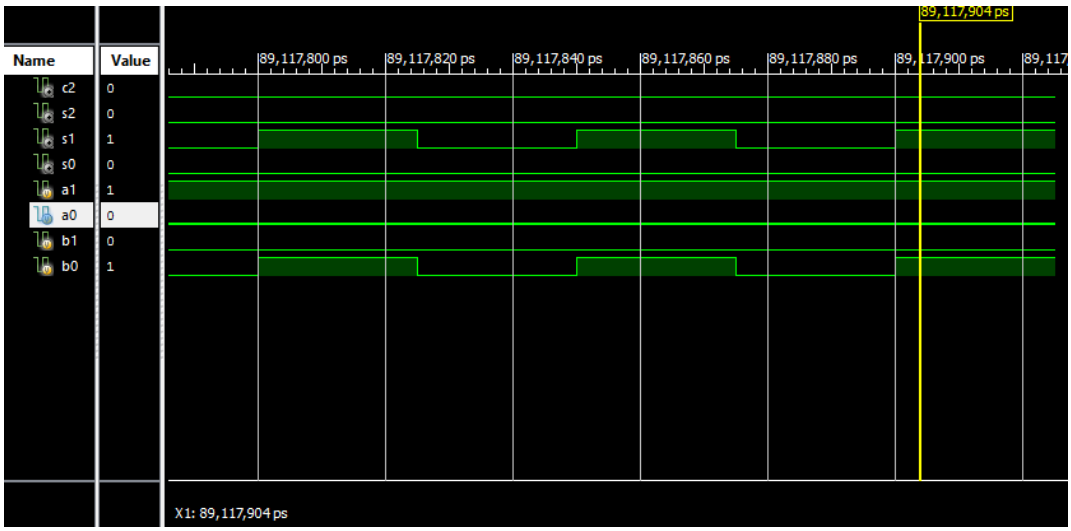

Figure 9: Simulation result for 2 × 2 bit VM.

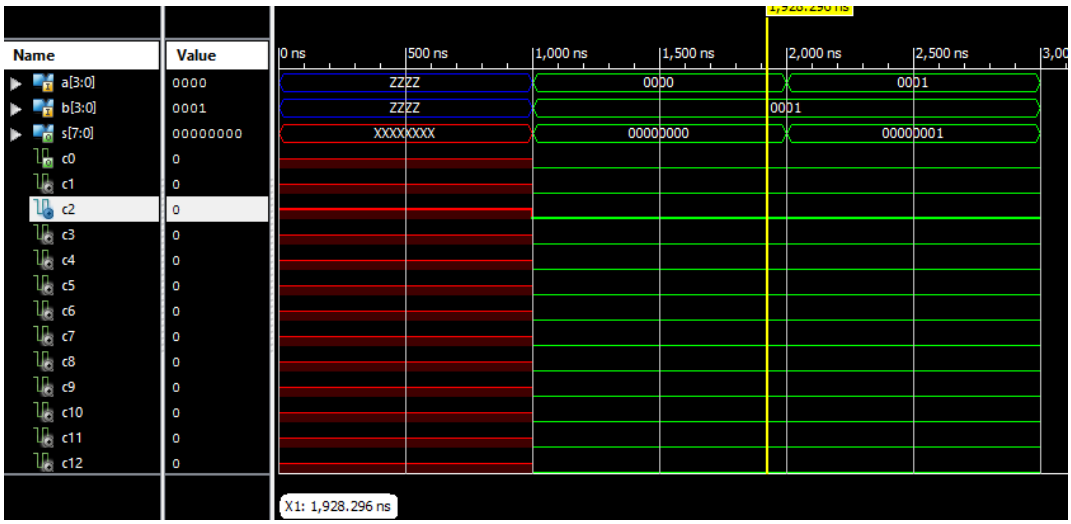

Figure 10: Simulation result for 4 × 4 bit VM.

Selected Device	3s4000fg208-5(Spartan 3)
Number of Slices	2 out of 2854 (0%)
Number of 4 input LUTs	4 out of 7168 (0%)
Number of IOs	8
Number of bonded IOBs	8 out of 151 (5%)

Table 2: Device utilization summary for 2 × 2 bit VM.

Selected Device	3s4000fg208-5(Spartan 3)
Number of slices	23 out of 3584 (0%)
Number of 4 input LUTs	42 out of 7168 (0%)
Number of IOs	17
Number of bonded IOBs	17 out of 141 (12%)

Table 3: Device utilization summary for 4 × 4 bit VM.

in terms of their respective power consumption and delay. Power consumption, delay generated, device utilization summaries for each of above mentioned is shown in Table 1. It can be observed that delay in our designed circuit is much lesser for 4 bit VM, compared to power delay analysis of CMOS multipliers using Vedic algorithm [8]. Similarly other parameters are obtained to be nearly equal to other design methodologies [7,8]. It has been seen that power consumption can reduced in the implementation of any logic circuit using reversible logic gate. Here, author simulated & synthesized the logic circuits using Xilinx software. Also, author implemented them by using peres gates, but other reversible gates can also be used for this purpose. Proposed circuits have applications in digital circuits like reversible processor, quantum computing, etc.

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