Journal of
Electrical & Electronic Systems

Chaudhry, J Elec Electron 2012, 1:1
DOI: 10.4172/2167-101X.1000e103

Editorial Open Access

Current Challenges in Scaling of MOS Technology

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Since the invention of the transistor in 1947, the technology has progressed smoothly resulting in reliable, handy, cheap and energy-efficient products. This has been made possible with the continuous scaling down of the transistor into the sub-micron and then to nanoscale region for the need of more compactness and speed. The pace of scaling down process has been retarded due to some adverse effects occurring at nanometer scale posing some tough challenges. One of the biggest challenges is the failure of classical physics, at nanometer scale. The failure is caused due to inversion layer quantization in the traditional silicon substrates and the increasing gate oxide tunneling currents. The inversion layer quantization is a serious issue as it decreases the drain current and the gate capacitance in a traditional planar transistor. The direct gate oxide tunneling increases the static power consumption in a transistor, thus putting a constraint on the power budget of a transistor. Several solutions have been proposed to counter these problems in nanoscale transistors. One of the solutions is the use of strain silicon substrate instead of crystalline pure silicon. The strain silicon technology is uniaxial and biaxial. In uniaxial technology, the mechanical stress is applied across the MOSFET at the gate or from the source and drain compression. The biaxial technology is obtained by doping germanium into silicon substrate. The strain silicon technology is promising but the integration of such technology with the conventional CMOS technology is still debatable in industry and academia. However, Intel introduced strained silicon technology in its products in the year 2003.

To tackle the gate oxide tunneling problem, high-k materials are proposed. These materials include hafnium oxide, lanthanum oxide etc. These materials look promising for 45 nm technologies but some issues like integration with conventional technology, defects, decreasing carrier mobility etc. have posed a bigger challenge on the alternatives proposed for sub 45 nm technologies. However, high-k/metal gate technology was introduced by Intel in the year 2007.

The other issue which poses a serious challenge to MOSFET scaling is the interconnect technology for nanoscale transistor wiring. The scaling in the resistance and associated capacitance is increasing delay in the on-chip wiring. The solution proposed is the use of low k materials as interconnect isolators using even air-gap technology has also been initiated till 22 nm.

The other challenge is the development of computational and fabrication industry for such technology. To develop TCAD tools for such complex devices and processes, newer models are needed to understand the physics at nanometer scale. The fabrication issue is also a ticklish issue with the development of lithography technology for such scales. This involves the cost, experience and time to cater fully to the challenges posed by this technology.

Now, in 2011, actual fabrication of silicon transistors at 22 nm technology in three dimensions has been initiated by Intel by introducing tri-gate transistor, in which the transistor channel is controlled in three directions. This type of transistor has better control of the current flow rather than the conventional, planar transistors.

So, the prime concern is to develop a suitable technology for scaling down further of the transistors or some innovations are required in the form of carbon nano-tube based transistors or other unconventional technology which will altogether replace the traditional MOSFET which has been ruling the electronics market for the last six decades.

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Received January 27, 2012; **Accepted** January 30, 2012; **Published** February 02, 2012

Citation: Chaudhry A (2012) Current Challenges in Scaling of MOS Technology. J Elec Electron 1:e103. doi:10.4172/2167-101X.1000e103