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Adaptive Decision Feedback Equalization for Multi-Gbps Serial Links: Challenges and Opportunities

Fei Yuan*

Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada

Abstract

This editorial briefly examines challenges in design of adaptive decision feedback equalizers for multi-Gbps serial links. The state-of-the-art of serial links over wire channels is briefly reviewed. The impairment of wire channels at high frequencies and their effect on the performance of serial links are examined. It is followed with a close examination of channel equalization techniques to combat inter-symbol interference. Challenges and opportunities in design of adaptive feedback equalizers including timing constraints, power consumption, adaptive references for error generation and thresholds for logic state determination, data-DFE, eye-opening monitor DFE, and edge-DFE, floating tap DFE are examined.

Introduction

Data-intensive applications such as video streaming, cloud computing, and virtual presence devices require data to be transmitted among chips, modules, and chassis via serial copper channels at tens of giga-bit-per-second (Gbps), as shown in Table 1. The data rate of these links is limited by inter-symbol interference (ISI) arising from channel impairment such as finite bandwidth, reflection, and crosstalk [1]. Al-though low-loss channels and low-reflection vias/connectors are highly desirable, they are costly. Combating the effect of channel imperfection by means of channel equalization is proven to be the most robust, effective, and economical. This editorial briefly examines difficulties encountered in design of adaptive decision feedback equalizers for multi-Gbps serial links. In addition, it browses through recent developments that overcome these difficulties and challenges that are yet to be conquered.

Channel Equalization

ISI can be minimized by either boosting the high-frequency components or attenuating the low-frequency components of data symbols at transmitter end prior to data transmission. This is known as pre-emphasis [12-15]. Pre-emphasis is usually realized using a finite impulse response (FIR) filter with its zeros canceling out the poles of the channels ideally [16]. The order of pre-emphasis filters is low, typically 2~3 revealing that channels can be adequately modeled using low-order low-pass systems provided that the effect of reflection and crosstalk is not accounted for [17,18]. Since the exact characteristics of channels are typically unknown a priori, the optimal coefficients of pre-emphasis FIR filters cannot be determined precisely. As a result, pre-emphasis alone is incapable of achieving total channel equalization. The deployment of pre-emphasis is also hindered by the crosstalk between channels and neighboring devices if the high-frequency components of data symbols are overly amplified or the deterioration of signal-to-noise ratio if the low-frequency components of data symbols are overly attenuated. Another limitation of pre-emphasis is its inability to eliminate ISI caused by reflection and crosstalk, which is significant at high data rates.

Far-end channel equalization combats ISI by either amplifying the high-frequency components of received data symbols or removing post-cursors by subtracting estimated post-cursors from data symbols. The former is known as continuous-time linear equalization (CTLE) while the latter is termed nonlinear equalization. Since the effect of the imperfection of channels is entailed in data symbols received at the far end of the channels, post-equalization can be adjusted objectively to eliminate the effect of the impairments of the channels so as to achieve better channel equalization. This differs fundamentally from pre-emphasis, which equalizes channels blindly unless a back channel that conduits the performance of pre-emphasis measured at the far end of the channel back to the transmitter exists. Although ideally CTLE is capable of canceling out the poles of the channels so as to achieve full channel equalization, the amplification of the high-frequency components of incoming data symbols, which are often corrupted by noise and disturbances, will worsen noise and disturbances subsequently the performance of data links. It is also difficult to obtain a large gain of CTLE at high frequencies. As a result, CTLE with only a moderate gain is typically deployed. Most channel equalization tasks, especially the

Ref.	Tech. [nm]		Channel loss [dB]	Data rate [Gbps]
Amirkhany *et al.* (2012) [2]	40		-10	16
Kaviani *et al.* (2012) [3]	40		-15	20
Cui *et al.* (2012) [4]	40		-20	23
Toifl *et al.* (2012) [5]	32	SOI	-27	12.5
Toifl *et al.* (2012) [6]	32	SOI	-36	30
Bulzacchelli *et al.* (2012) [7]	32	SOI	-35	28
G. Gangasani *et al.* [8] (2014)	32	SOI	-30	32
J. Savoj *et al.* [9] (2012)	28		-33	12.5
R. Navid *et al.* [10] (2015)	28		-20	40
P. Francese *et al.* [11] (2014)	22	SOI	-34	16

Table 1: Data rates of serial links over wire channels. Channel loss is measured at half baud-rate frequency.

***Corresponding author:** Fei Yuan, Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada, Tel: 41697950005; E-mail: fyuan@ryerson.ca

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removal of reflection/crosstalk-induced ISI, are usually left to nonlinear equalizers [18-21]. As CTLE is typically con-figured differentially with RC source degeneration feedback where the capacitor shorts the resistor at high frequencies thereby boosting gain at high frequencies, CTLE is subject to the effect of a mismatch-induced input offset voltage. As data symbols are severely attenuated when reaching the far end of channels, the input offset voltage of CTLE can become comparable to the voltage of received data symbols, mandating the compensation of the effect of input offset voltage in CTLE [22,23]. Unlike CTLE, nonlinear equalization removes post-cursors by subtracting estimated post-cursors from incoming data symbols directly. The estimate of a post-cursor is obtained by multiplying the corresponding past decision of the slicer with an appropriate coefficient, i.e., a tap coefficient. The most widely used nonlinear equalization is decision feedback equalization proposed by Austin in 1967 [24]. A distinct characteristic of DFE is that DFE does not deteriorate crosstalk as no amplification of the high-frequency components of incoming data symbols is performed. In addition, since the taps of DFE can be adjusted in accordance with the response of channels, which entails the effect of the impairment of the channels, DFE is not only capable of eliminating ISI caused by finite channel bandwidth, it also has the ability to remove ISI caused by reflection and crosstalk, a distinct characteristic not possessed by pre-emphasis. DFE is therefore the most robust and widely used channel equalization technique.

Challenges and Opportunities

Timing constraints

DFE is a negative feedback system. The most widely used DFE is based on least mean square (LMS) principle. LMS DFE obtains desired tap coefficients by minimizing the power of the difference between the equalized and desired data symbols at the center of data eyes. For high-speed serial links, only sign-sign least-mean-square (SS-LMS), which only uses the sign rather actual value of the difference between equalized and desired data symbols, is used. The operation of a generic SS-LMS DFE includes data slicing that generates the signed difference (error) between equalized data symbols (the input of the slicer) and desired data symbols (the output of the slicer), the multiplication of tap coefficients with the past decisions of the slicer, and the subtraction of DFE taps from incoming data symbols. These operations must be completed in one unit interval (UI).

The need for positive feedback in slicers so as to yield an output with a large voltage swing sets the lower bound of the latency of the slicers. Most slicers are based on the architecture of sensing amplifiers, which consist of a differentially configured sensing stage and a positive feedback latch output stage. In order to meet timing requirements, loop unrolling emerged as an effective means to avoid the difficulties encountered in lowering the latency of slicers [25-28]. DFEs with data rates in the vicinity of 10 Gbps typically employ only first-order loop unrolling, i.e., loop unrolling for tap 1 only.

High-order loop unrolling, i.e., loop unrolling for for taps 1~3, has also been used in order to meet timing constraints when data rate reaches tens of Gbps. This, however, is at the cost of exponentially increased silicon and power consumption [5,6,29]. To relax the timing constraints and lower the power consumption of remaining taps, half-rate or even quarter-rate approaches have been used [5,6,16,26,29]. This approaches trades silicon for power consumption.

In addition to data slicing, both multiplication and summation operations are also needed in DFE and these operations must be completed in less than one UI. Each DFE tap to be subtracted from incoming data symbols is the product of a tap coefficient, which is an analog quantity, and the past decision of the slicer, which is a digital quantity. To perform multiplication, fully differential current-steering multipliers with the tail current representing the tap coefficient and current-steering signal from the output of the slicer are widely favored [30-32]. The summation block performs the subtraction of DFE taps from incoming data symbols. The large capacitance encountered at the tap summing node of the summation block, arising from the large number of DFE taps, has a detrimental impact on the speed of the summation block [26]. To minimize the delay, current-mode summation is widely favored over its voltage-mode counterpart due to the intrinsic advantages of current-mode circuits [33]. In addition to delay, as the output of the summation block is also the input of the slicer, a large output voltage of the summation block is critical in minimizing slicer error. Increasing the dimension of the input transistors of the summation block, though improving the current flowing to the load of the summation block subsequently the output voltage swing of the block, also reduces the speed due to a large input capacitance. Lowering the load resistance of the summation block, although reducing the time constant of the summing node subsequently the delay of the summation block, also lowers the input voltage of the slicer. One effective way to speed up the summation block without reducing the load resistance is to use inductor peaking, i.e., replacing the load resistors of the summation block with inductors [19,34]. Though effective, the high cost of on-chip spiral inductors needs to be justified. Current-integrating summation with resistor loads offers the advantage of low power consumption [35-37]. The replacement of resistor loads with PMOS transistors loads that operate in an ON/OFF mode further lowers the power consumption [30-32]. The speed of current-integrating summation can be further increased by re-placing current feedback taps with capacitive charge feedback [5,6,29]. To further reduce power consumption, switched-capacitor summers were proposed [32]. Since complex clock schemes are needed, switched-capacitor summers are typically used to perform the summation of the first-tap with the rest of the taps implemented using the current-integrating approach.

Power consumption

Increasing power consumption in general helps speed up circuits. The aggressive scaling of CMOS technology has granted designers the permission to trade silicon for power reduction and speed improvement. This is largely achieved using approaches similar to time-interleaving where the rate of the speed and power reduction of time-interleaved blocks is approximately the same as that of silicon consumption increase. Typical examples in Gbps serial links are loop unrolling for the first few taps and half-rate or even quarter-rate clocking for remaining taps. Loop unrolling is geared towards meeting the timing constraints whereas half-rate and quarter-rate clocking is aimed at lowering power consumption. Power-speed trade-off also exists in current-mode logic, which is widely used in serial links due to their advantages of high-speed operation and low switching noise. Recently charge-steering emerged as a promising technique to significantly reduce both the power consumption and the latency of the building blocks of digital logic [38-40]. As compared with current-mode logic, charge-steering logic replaces the load resistors and the tail current source of current-mode logic with clocked switches and steer the charge between device capacitors at the output nodes and that at the common-source node. Unlike switched-capacitor networks that require a total charge transfer between clock phases so that the performance of these networks only depends on capacitance ratios, the amount of charge transfer of charge-steering circuits per clock phase is controlled by the input voltage. As

a result, by adjusting the ratio of capacitors involved, a tunable voltage gain can be obtained. The small time constant formed by switches and capacitors enables a rapid charge transfer so as to achieve a high-speed operation. The elimination of the tail current source and load resistors also greatly lowers power consumption. As demonstrated in Ref. [39], a 20-fold reduction in the power consumption of a clock and data recovery circuit was obtained.

Adaptive references and thresholds

The variation of the characteristics of channels, the uncertainty in the arrival of reflected signals, and the randomness of crosstalk from neighboring devices require that the number of the taps and the value of the coefficients of the taps of DFE be set adaptively. In SS-LMS DFE, although theoretically the error signal used by DFE algorithms is the sign of the difference between equalized data symbols, which is the input of the slicer, and the desired data symbols, which is the output of the slicer, since the output of the slicer is digital while the input of the slicer is analog, the sign of their difference will always be either positive or negative, rather than be toggled between 1 and -1. This difficulty can be overcome by comparing equalized data symbols with their desired voltages $V_{ref;1}$ for data 1 and $V_{ref;0}$ for data 0. The logic state of data symbols is determined by comparing equalized data symbols with a threshold voltage V_T, typically set to the common-mode voltage of the data symbols.

For DFE with 4 PAM signaling, the error signals used by DFE are generated by comparing incoming data symbols with their desired voltages $V_{ref;00}$ for data bits 00, $V_{ref;01}$ for data bits 01, $V_{ref;10}$ for data bits 10, and $V_{ref;11}$ for data bits 11. The data bits of incoming data symbols are determined by comparing the data symbols with threshold voltage $V_{T;01\ 00}$ defining the border between data symbols 00 and 01, $V_{T;10\ 01}$ defining the border between data symbols 01 and 10, and $V_{T;11\ 10}$ defining the border between data symbols 10 and 11. Since both the references and thresholds with which incoming data symbols compare are not known a priori and varies with data rate and the characteristics of channels, they should be set in accordance with data rate and the characteristics of channels in an adaptive manner, similar to tap coefficients. For DFE with 2 PAM signaling, a total of 4 adaptive algorithms, one for tap coefficients, one for threshold V_T, two for references $V_{ref;1}$ and $V_{ref;0}$ are needed, resulting in an excessive amount of silicon and power consumption.

Silicon and power consumption will become prohibitively high for DFE with 4 PAM signaling if every reference for error generation and every threshold for logic state determination are to be set adaptively [41-44,27]. It was shown in Ref. [44] that the number of references can be reduced from 4 to 1 with the chosen reference for error generation corresponding to one of the four data symbols. The reference is updated only on the arrival of the corresponding data symbol. This approach trades performance for receiver simplicity. A critical piece of information that is missing is the relation between the chosen reference and the performance of DFE, specifically, what are the factors that dictate the choice of the reference and which reference gives the best performance? Also, what is the performance compromise if only one reference is used?

Data-DFE, eye-opening monitor DFE, and Edge-DFE

Unlike SS-LMS data-DFE, eye-opening monitor (EOM) adaptive DFE hereafter referred to as EOM-DFE uses a pre-defined minimum data eye as the benchmark to guide the search for desired tap coefficients [45-49]. Since equalization is activated only when data eyes are smaller than the pre-defined minimum data eye and ceased if data eyes exceed the pre-defined minimum data eye, EOM-DFE is more power-efficient. Similar to data-DFE, which has no explicit constraint imposed on data jitter, EOM-DFE suffers from the lack of a tight constraint on data jitter. For example, a one-dimensional EOM only has a vertical eye-opening constraint and does not have any constraint on data jitter. Although a two-dimensional EOM has a constraint on data jitter, the jitter constraint conflicts with vertical eye-opening constraint. Hexagon EOM tightens jitter constraint without sacrificing vertical eye-opening, however, at the expense of more silicon and power consumption [50]. Data-dependent jitter, a prominent form of the deterministic jitter of data symbols, arises from the impairment of channels and is a major contributor to ISI [51]. Transition (edge) information, normally used for recovering clock embedded in data, was also utilized to generate error information used by DFE [52]. This DFE differs from data-DFE and EOM-DFE and is known as edge-DFE [53]. Edge-DFE searches for desired tap coefficients by minimizing the power of timing error (jitter) of data eyes. Since timing error information is readily available in phase-picking clock recovery [33], no additional cost is encountered in edge-DFE. As compared with data-DFE, edge-DFE possesses a number of attractive characteristics including reduced data-dependent jitter and relaxed CTLE gain constraint [53]. This, however, is at the cost of reduced vertical eye-opening. To eliminate this drawback, both edge-DFE and data-DFE were employed simultaneously in Ref. [16] so as to utilize the advantages of both data-DFE and edge-DFE. In addition, the strength of each DFE can be adjusted objectively and independent of each other. Information that is critically needed is the theory that governs the assignment of the weighting factors between data-DFE and edge-DFE so as to yield the optimal performance.

As phase-picking based data recovery is intrinsically sensitive to errors in data sampling unless a multiple samples per symbol time are taken and a digital filtering mechanism such as majority-voting is employed to filter out irregular samples. Similarly, phase-tracking based data recovery is also prone to errors in samples as it solely relies on data samples at the center of data eyes. Integration-based data recovery, which determines the logic stage of incoming data by integrating the data over one symbol time and comparing the result with a pre-defined threshold, is preferred over their sampling counterparts [54-56]. The simultaneous deployment of data-DFE and edge-DFE will maximize both the horizontal and vertical eye-openings of data eyes thereby maximizing the difference between logic-1 and logic-0 subsequently BER.

Floating tap DFE

For severely dispersive channels, a large number of taps are needed in order to remove post-cursors, resulting in both an excessive amount of power and silicon consumption, and a large capacitance at the input of the slicer, which imposes a great challenge on meeting the timing constraint. When impedance discontinuities typically occurring at vias and connectors exist in channels, reflection-induced post-cursors are generated. These post-cursors have two distinct characteristics: Location uncertainty and amplitude uncertainty. Often they reside at locations far away from the main cursor with a large number of insignificant post-cursors in between. If generic DFE is used, the equalization of these channels requires a large number of taps even though those corresponding to the insignificant post-cursors between the main cursor and reflection-induced post-cursors contribute negligibly to the overall equalization of channels. As a result, not only a significant amount of silicon and power is wasted, an exceedingly large capacitor is also introduced at the input of slicers. To address this problem, floating-tap DFE dynamically locates reflection-induced

post-cursors and places taps only at the location of the reflection-induced post-cursors. The number of the taps can be significantly reduced [20,21,57,58]. Despite of its importance, a very limited number of studies on floating-tap DFE are available. More research is clearly warranted on how to dynamically place taps to the location where large reflection-induced post-cursors reside.

Conclusions

The impairment of wire channels and its impact on multi-Gbps serial links were examined. It was followed with a close examination of channel equalization techniques, in particular, pre-emphasis and post-equalization, to combat inter-symbol interference. The difficulties encountered in design of adaptive decision feedback equalizers were investigated and recent developments that overcome these difficulties were studied. Challenges that are yet to be conquered were explored.

References

1. Johnson H, Graham M (2003) High Speed Digital Design: A Handbook of Black Magic. Upper Saddle River, New Jersey: Prentice-Hall.
2. Amirkhany A, Kaviani K, Abbasfar A, Fazeel S, Beyene W, et al. (2012) A 4.1-pJ/b, 16-Gb/s coded differential bidirectional parallel electrical link. IEEE J. Solid-State Circuits 47: 3208-3219.
3. Kaviani K, Wu T, Wei J, Amirkhany A, Shen J, et al. (2012) A tri-modal 20-Gbps/link differential/DDR3/GDDR5 memory interface. IEEE J. Solid-State Circuits 47: 926-937.
4. Cui D, Raghavan B, Singh U, Vasani A, Huang Z, et al. (2012) A dual-channel 23-Gbps CMOS transmitter/receiver for 40-Gbps RZ-DQPSK and CS-RZ-DQPSK optical transmission. IEEE Solid-State Circuits 47: 3249-3260.
5. Toifl T, Menolfi C, Ruegg M, Reutemann R, Dreps D, et al. (2012) A 2.6 mW/Gb/s 12.5 Gbps RX with 8-tap switched-capacitor DFE in 32 nm CMOS. IEEE J. Solid-State Circuits 47: 897-910.
6. Thomas T, MichaelR, RajeshI ,ChristianM,MatthiasB, et al. (2012) A 3.1 mW/Gb/s 30 Gbps quadrater-rate triple-speculation 15-tap SC-DFE RX data path in 32 nm CMOS. Symp. Circuits Dig. Tech Papers pp. 102-103.
7. Bulzacchelli J, Menolfi C, Beukema T, Storaska D, Hertle J, et al. (2012) A 28-Gb/s 4-tap FFE/15-tap DFE serial link transceiver in 32-nm SOI CMOS technology. IEEE J. Solid-State Circuits 47: 3232 - 3248.
8. Gangasani G, Hsu C, Bulzacchelli J, Beukema T, Kelly W, et al. (2014) A 32 Gb/s backplane transceiver with on-chip AC-coupling and low latency CDR in 32 nm SOI CMOS technology. IEEE J. Solid-State Circuits 49: 2474 - 2489.
9. Savoj J, Hsieh K, Upadhyaya P, An F, Bekele A, et al. (2012) A wide common-mode fully-adaptive multi-standard 12.5 Gb/s backplane transceiver in 28 nm CMOS. Symp. VLSI Circuits Dig. Tech. Papers pp: 104-105.
10. Navid R, Chen E, Hossain M, Leibowitz B, Ren J, et al. (2015) A 40 Gb/s serial link transceiver in 28 nm CMOS technology. IEEE J. Solid-State Circuits 50: 814-827.
11. Francese P, Toifl T, Buchmann P, Brandli M, Menolfi C, et al. (2014) A 16 Gb/s 3.7 mW/Gb/s 8-Tap DFE receiver and baud-rate CDR with 31 kppm tracking bandwidth. IEEE Solid-State Circuits 49: 2490 - 2502.
12. Fiedler A, Mactaggart R, Welch J, Krishnan S (1997) A 1.0625 Gbps transceiver with 2x-oversampling and transmit signal pre-emphasis. IEEE Int'l Solid-State Circuits Conf., Dig. Tech. Papers pp: 238-239.
13. Dally J, Poulton J (1997) Transmitter equalization for 4-Gbps signaling. IEEE Micro 17: 48-56.
14. Zhao Z, Wang J, Li S, Chen J (2007) A 2.5-Gb/s 0.13 m CMOS current mode logic transceiver with pre-emphasis and equalization. Proc. Int'l conf. ASIC pp: 368-371.
15. Kao S, Liu S (2010) A 20-Gb/s transmitter with adaptive pre-emphasis in 65-nm CMOS technology. IEEE Trans. Circuits Syst. II 57: 319-323.
16. Wong K, Chen E, Yang C (2008) Edge and data adaptive equalization of serial-link transceivers. IEEE J. Solid-State Circuits 43: 2157-2169.
17. Lee M, Dally W, Farjad-Rad R, Senthinathan H NgR, Edmondson J (2003) CMOS high-speed I/Os- present and future. Proc. Int'l Conf. Computer Design pp: 454-461.
18. Balan V, Caroselli J, Chern J, Chow C, Dadi R, et al. (2005) A 4.8-6.4-Gb/s serial link for backplane applications using decision feedback equalization. IEEE J. Solid-State Circuits 40: 1957-1967.
19. Ying Y, Liu S (2011) A 20Gb/s digitally adaptive equalizer/DFE with blind sampling. IEEE Int'l Solid-State Circuits Conf. Dig. Tech. Papers pp: 444-446.
20. Zhong F, Quan S, Liu W, Aziz P, Jing T, et al. (2011) A 1.0625-to-14.025 Gb/s multimedia transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS. IEEE Int'l Solid-State Circuit Conf. Dig. Tech. Papers pp: 348-349.
21. Zhong F, Quan S, Liu W, Aziz P, Tai J, et al. (2011) A 1.0625 - 14.025 Gb/s multi-media transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS. IEEE J. Solid-State Circuits 46: 3126-3139.
22. Hidaka Y, Gai W, Horie T, Jiang J, Koyanagi Y (2009) A 4-channel 1.25-10.3 Gb/s backplane transceiver macro with 35 dB equalizer and sign-based zero-forcing adaptive control. IEEE J. Solid-State Circuits 44: 3547-3559.
23. Kim B, Liu Y, Dickson T, Bulzacchelli J, Friedman D (2009) A 10-Gb/s compact low-power serial I/O with DFE-IIR equalization in 65-nm CMOS. IEEE J. Solid-State Circuits 44: 3526-3538.
24. Austin ME (1967) Decision feedback equalization for digital communication over dispersive channels. IEEE Int'l Research Laboratory of Elec-tronics Technical Report 461.
25. Krishna K, Yokoyama-Martin D, Caffee A, Jones C, Loikkanen M, et al. (2005) A multi-giga-bit backplane transceiver core in 0.13- m CMOS with a power-efficient equalization architecture. IEEE J. Solid-State Circuits 40: 2658-2666.
26. Beukema T, Sorna M, Selander K, Zier S, Ji B, et al. (2005) A 6.4-Gb/s CMOS SerDes core with feed-forward and decision-feedback equalization. IEEE J. Solid-State Circuits 40: 2633-2645.
27. Bulzacchelli J, Meghelli M, Rylov S, Rhee W, Rylyakov A, et al. (2006) A 10-Gb/s 5-tap DFE/4-tap FFE transceiver in 90 nm CMOS technology. IEEE J. Solid-State Circuits 41: 2885-2900.
28. Leibowitz B, Kizer J, Lee H, Chen F, Ho A, et al. (2007) A 7.5Gb/s 10-tap DFE receiver with first tap partial response, spectrally gated adaptation, and 2nd-order data-filtered CDR. IEEE Int'l Solid-State Circuits Conf. Dig. Tech. Papers pp: 228 -599.
29. Toifl T, TMM Ruegg, Inti R, Menolfi C, Brandli M, et al. (2012) A 3.1 mW/Gbps 30 Gbps quarter-rate triple-speculation 15-tap SC-DFE RX data path in 32 nm CMOS. Symp. VLSI Circuits Dig. Tech. Papers pp: 102-103.
30. Dickson T, Bulzacchelli J, Friedman D (2008) A 12 Gb/s 11 mW half-rate sampled 5-tap decision feedback equalizer with current-integrating summers in 45 nm SOI CMOS technology. Symp. VLSI Circuits Dig. Tech. Papers pp: 58-59.
31. Bulzacchelli J, Dickson T, Deniz Z, Ainspan H, Parker B, et al. (2009) A 78 mW 11.1Gb/s 5-tap DFE receiver with digitally calibrated current-integrating summers in 65nm CMOS. IEEE Int'l Solid-State Circuits Conf. Dig. Tech. Papers pp: 368 -369.
32. Payandelhnia P, Abbasfar A, Sheikhaei S, Forouzandeh B, Nan-bakhsh K, et al. (2011) A 4 mW 3-tap 10 Gb/s decision feedback equalizer. Proc. IEEE Mid-West Symp. Circuits Syst pp: 1-4.
33. Yuan F (2007) CMOS current-mode circuits for data communications. Springer, New York.
34. Ibranhim S, Razavi B (2011) Low-power CMOS equalizer design for 20-Gb/s systems. IEEE J. Solid-State Circuits 46: 1321- 1336.
35. Park M, Bulzacchelli J, Beakes M, Friedman D (2007) A 7 Gb/s 9.3 mW 2-tap current-integrating DFE receiver. Digest of Technical Papers, IEEE International pp: 230-231.
36. Bulzacchelli J, Rylyakov A, Friedman D (2007) Power-efficient decision-feedback equalizers for multi-Gb/s CMOS serial links. Proc. IEEE Radio Frequency Integrated Circuits Symp pp: 507 -510.
37. Dickson T, Bulzacchelli J, Friedman D (2009) A 12 Gb/s 11 mW half-rate sampled 5-tap decision feedback equalizer with current-integrating summers in 45-nm SOI CMOS technology. IEEE J. Solid-State Circuits 44: 1298-1230.

38. B. Razavi (2013) Charge steering: A low-power design paradigm. Proc. IEEE Custom Integrated Circuits Conf pp: 1-8.

39. Jung J, Razavi B (2013) A 25-Gb/s 5-mW CMOS CDR/Deserializer. IEEE J. Solid-State Circuits 48: 684-697.

40. Jun Won J, Razavi B (2015) A 25-Gb/s 5.8 mW CMOS equalizer. IEEE J. Solid-State Circuits 50: 515-526.

41. Stonick J, Wei G, Sonntag J, Weinlader D (2003) An adaptive PAM-4 5-Gb/s backplane transceiver in 0.25- m CMOS. IEEE J. Solid-State Circuits 38: 436 - 443.

42. Song B, Kim K, Lee J, Burm J (2013) A 0.18 m CMOS 10-Gb/s dual-mode 10-PAM serial link transceiver. IEEE Trans. Circuits Syst. I 60: 457-468.

43. Toifl T, Menolfi C, Ruegg M, Reutemann R, Buchmann P,et al. (2006) A 22-Gb/s PAM-4 receiver in 90-nm CMOS SOI technology. IEEE J. Solid-State Circuits 41: 954-965.

44. Stojanovic V, Garlepp AHoB, Chen F, Wei J, Tsang G, et al. (2005) Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery. IEEE J. Solid-State Circuits 40: 1012- 1026.

45. Chen L, Zhang X, Spagna F (2009) A scalable 3.6-5.2 mW 5-to-10 Gb/s 4-tab DFE in 32 nm. IEEE Int'l Solid-State Circuits Conf. Dig. Tech. Papers pp: 180-181.

46. Spagna F, Chen L, Deshpande M, Fan Y, Gambetta D, et al. (2010) A 78 mw 11.8Gb/s serial link transceiver with adaptive RX equalization and baud-rate CDR in 32 nm CMOS. IEEE Int'l Solid-State Circuits Conf. Dig. Tech. Papers pp: 366 -367.

47. Pozzoni M, Erba S, Viola P, Pisati M, Depaoli E et al. (2009) A multi-standard 1.5 to 10 Gb/s latch-based 3-tap DFE receiver with a SSC tolerant CDR for serial backplane communication. IEEE J. Solid-State Circuits 44: 1306-1315.

48. Noguchi H, Yoshida N, Uchida H, Ozaki M, Kanemitsu S, et al. (2008) A 40-Gb/s CDR circuit with adaptive decision-point control based on eye-opening monitor feedback. IEEE J. Solid-State Circuits 43: 2929-2938.

49. Bhatta D, Kim K, Gebara E, Laskar J (2009) A 10 Gb/s two dimensional scanning eye opening monitor in 0.18 m CMOS process. Proc. IEEE Int'l Microwave Symp. Digest pp: 1141-1144.

50. Al-Taee A, Yuan F, Ye A, Sadr S (2014) New 2d eye-opening monitor for gbps serial links. IEEE Transactions on Very Large Scale Integration Systems 22: 1209-1218.

51. Buckwalter A, Hajimiri A (2004) A 10 Gb/s data-dependent jitter equalizer. Proc. IEEE Custom Integrated Circuit Conf pp: 351-354.

52. Yamaguchi K, Sunaga K, Kaeriyama S, Nedachi T, Takamiya M, et al. (2008) 12 Gb/s duobinary signaling with x2 oversampled edge equalization. IEEE International Solid-State Circuits Conf., Dig. Tech. Papers pp: 70-71.

53. Brunn B (2004) Edge-equalized NRZ. Xilink Corporation.

54. Sidiropoulos S, Horowitz M (1997) A 700 Mb/s/pin CMOS signaling in-terface using current integrating receivers. IEEE J. Solid-State Circuits 32: 681-690.

55. Bae S, Chi H, Sohn Y, Lee J, Sim J, et al. (2009) A 2-Gb/s CMOS integrating two-tap DFE receiver for four-drop single-ended signaling. IEEE Trans. Circuits Syst. I 56: 1645-1656.

56. Gangasani G, Hsu C, Bulzacchelli J, Rylov S, Beukema T, et al. (2011) A 16-Gb/s backplane transceiver with 12-tap current integrating DFE and dynamic adaptation of voltage offset and timing drifts in 45-nm SOI CMOS technology. Proc. IEEE Custom Integrated Circuits Conference pp: 1 -4.

57. Lopez M, Singer A (2001) A DFE coefficient placement algorithm for sparse reverberant channels. IEEE Trans. on Communications 49: 1334-1338.

58. Aziz P, Kimura H, Malipatil A, Kotagiri S (2014) Shift register multi-phase based downbsampled floating tap DFE for serial links. Proc. IEEE Int'l Symp. Circuits and Systems pp: 2469-2472.