A 800 MHz-1.1 GHz 1.2 mW Delay Locked Loop with a Closed Loop Duty Cycle Corrector

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Abstract

In this paper a low power delay locked loop with a closed loop duty cycle corrector is proposed. The duty cycle corrector circuit is a dual loop circuit which receives a clock signal with 30%~70% duty cycle and generates a clock signal with 50% ± 2% duty cycle. The power consumption of the overall circuit is 1.2 mW. This circuit is fabricated in 0.18 um CMOS technology. Measurement results show that the RMS jitter of the proposed work is 4 ps at 1 GHz.

Keywords: Circuit; Jitter; Signal; Conventional; Synchronizing

Introduction

Delay locked loops are widely used for minimizing the clock jitter, clock skew reduction, synchronizing the clock signals, and generating accurate clock phase. DLL is a more stable circuit compared to PLL circuits. The reason behind this is that DLLs will only delay the input clock signal rather than generating a different frequency with a VCO. Therefore, it will not accumulate jitter and making it a more stable system.

Current mobile devices do not use conventional double data rate (DDR) DRAM. They use low power DDR (LPDDR) DRAM. LPDDR2 DRAM has been tested and commercialized with an operating frequency of up to 533 MHz [1]. This frequency will be increased in the next generation LPDDR interface. There are different reasons behind the clock signal specification variations. Driving strength of pull-up and pull-down paths of CMOS logic circuits are different, and this difference will increase with technology scaling. Also, PVT variation is another reason behind these variations.

Clock generators generate a reference clock with a 50% duty cycle. But duty cycle distortion will occur in the delay line of the DLL. Unfortunately, duty cycle distortion can even occur inside the DCC circuit itself [2,3]. Therefore, the use of a correction circuit like DCC is essential for DLLs being used in memory interface applications [4]. In addition to PVT variations, digital circuits suffer from different noise sources such as signal coupling and supply and ground noises. As the clock frequency increases, accurate DCC operation becomes more severe. This is because the timing margin tightens for high frequency operations.

In addition to these requirements, a low-power system is also very essential for mobile applications. Total power consumption is directly proportional to the number of building blocks operating at high frequency. Therefore, the number of blocks that operate at the same frequency as the clock signal must be reduced. These blocks for example include the delay line and phase detector (PD). Conventional DCC circuits fail to achieve this requirement and they even increase the delay line length. Therefore a DCC with a shorter delay line or a completely different structure is required for achieving low-power consumption and low cost.

In this work we use a low power mixed signal duty cycle correction circuit. This circuit is based on the conventional duty cycle corrector (DCC) and Pulse Width Control Loop (PWCL) structures [5-8]. These type of duty cycle correctors are previously used in frequency multipliers [9], Analog-to-Digital-Converters [10], and phase locked loops [11].

The rest of this paper is organized as followed. In Para 4 we talk about the circuit diagram of the proposed DLL and DCC. In Para 5 we talk about the simulation and measurement results. Finally, conclusions are provided in Para 6.

Circuit Structure

Block diagram of the proposed DLL with DCC is shown in Figure 1. In this structure DCC will receive the distorted clock signal and will generate a 50% duty cycle clock at the same frequency. This is done by the closed loop operation of the DCC circuit. The operation of the DCC circuit is as follows.

This PWCL includes a push-pull control stage which adjusts the pulse width of the CK in with respect to the control voltage. The push-pull control stage doubles the gain and accelerates the duty cycle correction. Unlike conventional structures, in this DCC two parallel control stages are used. This makes this structure a fully differential structure and the system will benefit from the advantages of a fully differential system like noise cancelation, etc. Besides, unlike the conventional DCC and PWCL structures, this fully differential control stage will use both falling and rising edges of the clock signal to create a 50% clock signal. This will improve the correction speed of this circuit. The circuit structure of the control stage is shown in Figure 2.

The second stage is a chain of clock buffers. This inverter chain is used to drive the heavy load of the output loads. The final stage is a
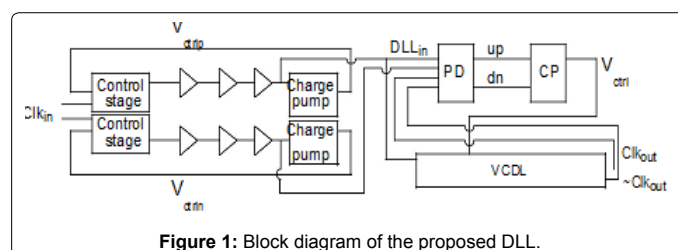

Figure 1: Block diagram of the proposed DLL.

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differential charge pump. This charge pump will generate two control signals (Vctrlp ,Vctrln), which each one corresponds to one of the control stages. One of these voltages will correspond to the falling edge of the input clock and the other one corresponds to the rising edge of the input clock signal. Circuit structure of the charge pump is shown if Figure 3.

The rest of the circuit is the same as all conventional DLLs. The 50% duty cycle clock signal will be fed to the phase detector (PD). Then based on the phase difference of the corrected clock and the feedback clock a series of pulses will be generated. These Up and Down pulses will be received at the input of the charge pump and will generate an analog signal to set the delay of the voltage controlled delay line (VCDL) circuit. Finally the output of the VCDL will be a duty cycle corrected and phase corrected clock signal. In this VCDL a low voltage delay cell is used to delay the 50% duty cycle clock signal. This structure is robust against duty cycle distortion. Circuit diagram of the delay cell is shown in Figure 4.

Simulation and Measurement Results

The proposed DLL is fabricated using 0.18 um CMOS technology. Supply voltage of the proposed circuit is at 1.8 V. In Figure 5 shows the transient simulation of the control signal. We didn't use any pad to measure this node because the capacitance of the pad and probes will load on this node and will affect the circuit behavior. This signal shows the transient behavior of the DCC circuit from beginning to locking. As you can see this signal is settled in less than 10 ns. In Figure 6 shows the simulation results of the DCC circuit. The input clock to this circuit is a 30% clock signal running at 900 MHz. The output of this circuit is a 50% clock signal running at the same frequency. Simulation
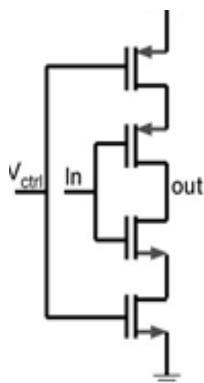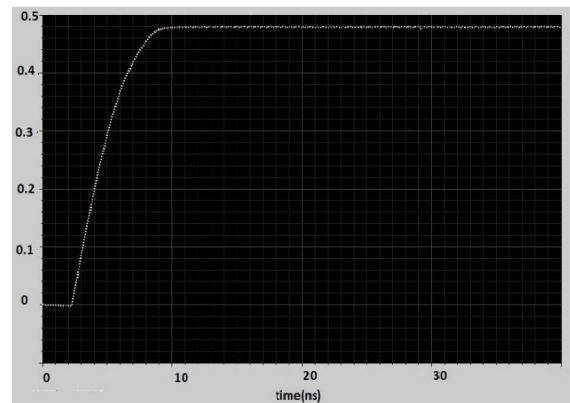

Figure 2: Control Stage
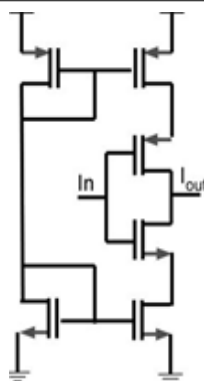
Figure 3: Charge pump circuit details (DCC).
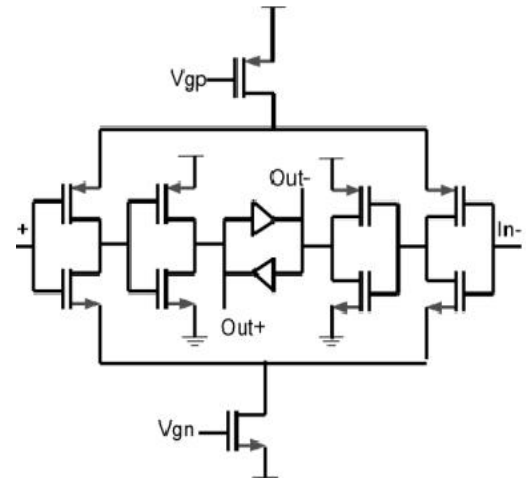

Figure 4: Delay cell used in VCDL.

Figure 5: Transient simulation results of the control signal.

results show that the proposed DCC alone can correct the clock signals ranging from 100 MHz to 1 GHz with a duty cycle of 30%~70%. The output of the circuit will be at the same frequency and has around 50% duty cycle. The power consumption of the DCC alone is about 0.8 mW. The corrected clock signal is fed to the DLL to lock on the phase of the duty cycle corrected clock signal. In Figure 7 shows the measurement results of the DLL. These measurements are done for the 800 MHz, and 1.1 GHz signals. As you can see from these results, the output signal is locked on the duty cycle corrected clock signal. The RMS jitter of the proposed structure is about 4 ps for a 1 GHz input clock signal. The power consumption of the overall circuit is 1.2 mW. Finally, Table 1 compares the circuit specifications of the proposed clock signal with conventional works.

Conclusions

A low power delay locked loop using a dual loop duty cycle corrector is presented. The duty cycle corrector circuit receives a 30%~70% duty cycle clock signal and generates a clock signal with 50% ± 2% duty cycle. The worst case power consumption of the overall circuit is 1.2 mW. This circuit is fabricated in 0.18 um CMOS technology. Measurement results show that the RMS jitter of the proposed work is 4 ps

at 1 GHz input clock. This circuit can be used in memory interface circuits where phase error and duty cycle error of the clock signal is an important factor.
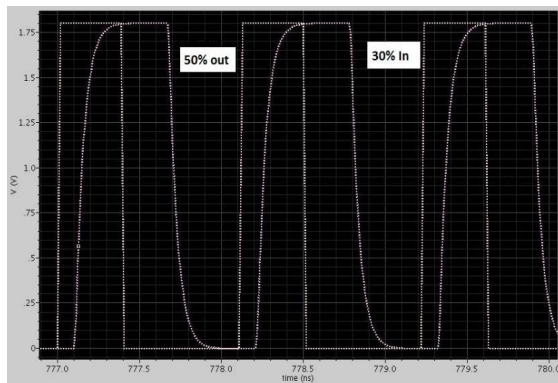
Figure 6: Input and output clock to DCC (900MHZ with 30% in, 900MHZ with 50% out).
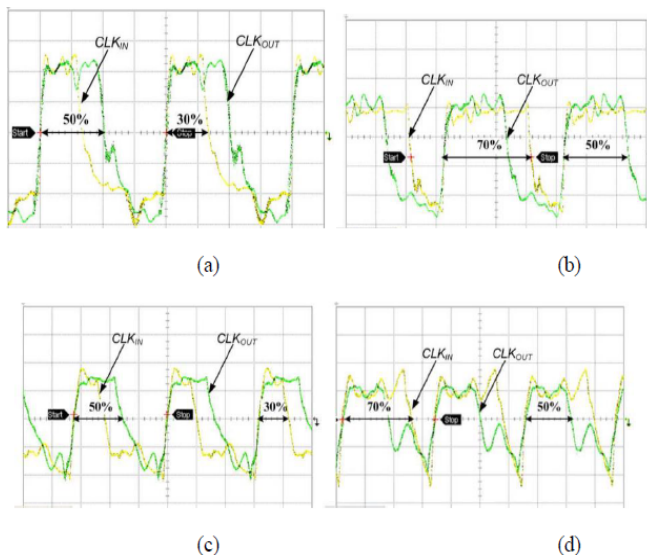
Figure 7: Measured waveforms with the input clock frequency and duty cycle at (a) 800MHz and 30% (b) 800MHz and 70% (c) 1.1GHz and 30% (d) 1.1GHz and 70%.

	This work	**[12]**	**[13]**	**[14]**
DCC	Closed loop	Closed loop	Closed-loop	Open-loop
Phase shift	Fixed phase	Multiphase	N/A	N/A
Frequency Range	800 MHz~1.1 GHz	333 MHz~800 MHz	N/A~1GHz	250 MHz~600 MHz
Correction range	30%~70%	23%~76%	15%~85%	40%~60%
Duty error	48%~52%	47.8%~49% @ 800 MHz	49.4%~50.6% @ 1 GHz	40.3%~50.7% @ 600 MHz
Power	1.2 mW	NA	8.2mW	10 mW
Supply	1.8 V	1.2 V	1.62 V	2.5 V
Process	0.18 um	0.13 um	0.18um	0.35 um

Table 1: Performance comparison with the state of the art.

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