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Physical design of quantum circuits in ion trap technology

Naser Mohammadzadeh
Shahed University, Iran

As feature sizes in CMOS technology shrink into the 10s of nanometer range, "quantum effects" should be managed. On the other hand, quantum effects such as superposition and entanglement are amplified and utilized in a quantum computer. Quantum circuits will have the capacity to solve some important mathematics and physics problems with fascinating asymptotic improvements. A quantum computer needs a large number of qubits and quantum gates to tackle a complex job such as factoring large numbers. To manage the complexity of the big systems, researchers divide the design flow into two main processes: logic synthesis and physical design. The logic synthesis process takes a design description as input and creates a technology-dependent gate-level netlist as output. On the other hand, the physical design process takes the output of the synthesis process and generates a specific layout constructed from the building blocks of the target technology. The finding of effective quantum algorithms in the mid-1990s and remarkable progress in quantum technologies motivate research on physical design. Extensive research has been concentrated on finding physical systems that can provide a large number of qubits while satisfying the scalability criteria. Ion traps have been the physical system of choice to demonstrate the most advanced quantum logic operations. A preliminary architecture has been proposed for assembling a large number of ions into a multiplexed trap on a chip. Much research has been done on the physical design of quantum circuits in ion trap technology. This speak talks about methodologies, architectures, optimization techniques, open issues, and future directions related to the physical design of quantum circuits in ion trap technology.

mohammadzadeh@shahed.ac.ir