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Design of insulators by atomic layer deposition for semiconductor devices

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Atomic layer deposition (ALD) technique has been widely investigated to achieve the requirements of atomic-level controllability and conformal growth on three-dimensional structure for a wide range of semiconductor application. Indeed, future scaling of Complementary Metal-Oxide-Semiconductor and charge trap flash memory require new materials as gate insulator and charge tarp layer, respectively. Ionic oxides such as Al_2O_3, TiO_2, and $(Ta/Nb)O_x$ have promising candidates because of a high dielectric constant (high-k) value and large band gap. We present characteristic of each layer and $Al_2O_3/(Ta/Nb)O_x/Al2O_3$ multi-layer fabricated by a low temperature process using ALD. The anatase TiO_2 and $(Ta/Nb)O_x$ thin films are negligible small charge and have significant high k value of about 30. We found that charge trap capacitors with $Al_2O_3/(Ta/Nb)Ox/Al_2O_3$ multi-layer show superior electrical properties and trapping mechanism of high-k layer as a charge trap layer.

Biography

Toshihide Nabatame received his PhD in Engineering in 1994 from Tokyo Institute of Technology and worked at Hitachi Ltd and Renesas Technology Co. He is manager of MANA Foundry in NIMS, Japan. His research interest is to find and fabricate functional devices with metal oxide thin film for future semiconductor region.

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