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Use of data analysis and TCAD simulations to understand the characteristics and reliability of high voltage MOS transistors

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High voltage metal-oxide-semiconductor (MOS) transistors are widely used in smart power management integrated circuits (IC), liquid-crystal display (LCD) drivers, and NAND flash memory periphery circuitry because of the compatibility to be integrated into standard complementary metal-oxide-semiconductor (CMOS) process. Because high voltage MOS transistors are operated under high voltage, breakdown voltage is a critical device parameter and hot-carrier induced device degradation is an important reliability concern. One key factor to affect breakdown voltage and hot-carrier induced device degradation is the process to fabricate drift region of the device. This paper reports analysis of breakdown voltage and hot-carrier induced device degradation in high voltage MOS transistors. The process to fabricate drift region of high voltage MOS transistors is varied to examine its impact on breakdown voltage and hot-carrier-induced device degradation. Not only experimental data but also technology computer-aided-design (TCAD) simulation results are analyzed to understand the underlying physical mechanisms. Our findings reveal that care should be taken in determining the fabrication process of drift region because a trade-off between breakdown voltage and hot-carrier induced device degradation is observed.

Biography

Jone F Chen received the PhD degree in Electrical Engineering from the University of California, Berkeley. He worked in the Department of Electrical Engineering and Institute of Microelectronics, National Cheng Kung University, Tainan, Taiwan for more than 15 years, where he is currently a Professor. He has published more than 50 papers in reputed journals.

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