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High-level synthesis through metaheuristics and LUTs optimization in FPGA devices

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Operations scheduling and lookup table (LUT) based technology mapping are fundamental problems of mapping designs onto an electronic device, such as a field programmable gate array. We present an approach to apply two optimizations consecutively. In first optimization, we apply several metaheuristic algorithms for multi-objective optimization at the high-level synthesis stage. And in second optimization, we realize reductions of LUTs at the logic synthesis stage. Several circuit designs are represented in a data flow graph (DFG) and the experiments are carried out on the standard Mediabench benchmark. In the first optimization, we compared NSGA-II, FEMO, HypE, IBEA, SPEA2 and WSGA. Results have an average improvement 14.06% in occupied area and 7.01% in power consumption. Then, optimized DFG schedules are converted into very high description language code using the Xilinx ISE design suite tool. Later, in the second optimization, the IMap algorithm is used to obtain combinational area reductions. Results show that 60% of the circuits are improved in comparison with the Xilinx ISE design suite.

Biography

Darian Reyes Fernandez de Bulnes is currently a PhD student in Engineering Sciences in the Department of Electrical and Electronics Engineering of the Tijuana Technological Institute, Mexico. He has received Bachelor's degree in Computer Science at the University of Computer Science in 2011 and Master's degree in Computer Science at the University of Havana in 2016, both in Cuba. His research areas include evolutionary computation, multi-objective metaheuristics and computer-aided design.

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