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Electrostatic discharge (ESD) protection for wireless communication IC's: challenges and solutions

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Electrostatic discharge (ESD) is one of the most prevalent threats to the reliability of electronic components. It is an event in which a finite amount of charge is transferred from one object (i.e., human body) to the other (i.e., microchip). This process can result in a very high current passing through the microchip within a very short period of time, and hence more than 35% of single-event catastrophic chip damages can be attributed to the ESD event. As such, designing on-chip ESD structures to protect integrated circuits against the ESD stress is a high priority in the semiconductor industry. The continuing scaling of complementary metal–oxide–semiconductor (CMOS) technology makes the ESD-induced failures even more prominent, and one can predict with certainty that the availability of effective and robust ESD protection solutions will become a critical and essential factor to the successful advancement and commercialization of the next-generation CMOS-based electronics. The development of radio frequency (RF) electronics went almost unnoticed until early 1980's because, unlike Si VLSI, there were no mass consumer markets for such applications. Recently, this has been changed drastically due to the explosive growth in the civil wireless communications and internets. The modern RF integrated circuits are typically operated in a voltage range of 2-4 V. This relatively low-voltage operation, together with the low tolerance of parasitic capacitance at the I/O pins and the continuing scaling in CMOS process, imposes certain challenges to the design and optimization of RF ESD protection solutions. An overview on the ESD sources, models, protection schemes, and testing will first be given in this talk. This is followed by presenting recent advancements and challenges on developing robust ESD protection solutions for modern low-voltage RF integrated circuits, as well as explorations and evaluations of ESD protection solutions in sub-28 nm and fin field-effect transistor (FinFET) CMOS technologies.

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